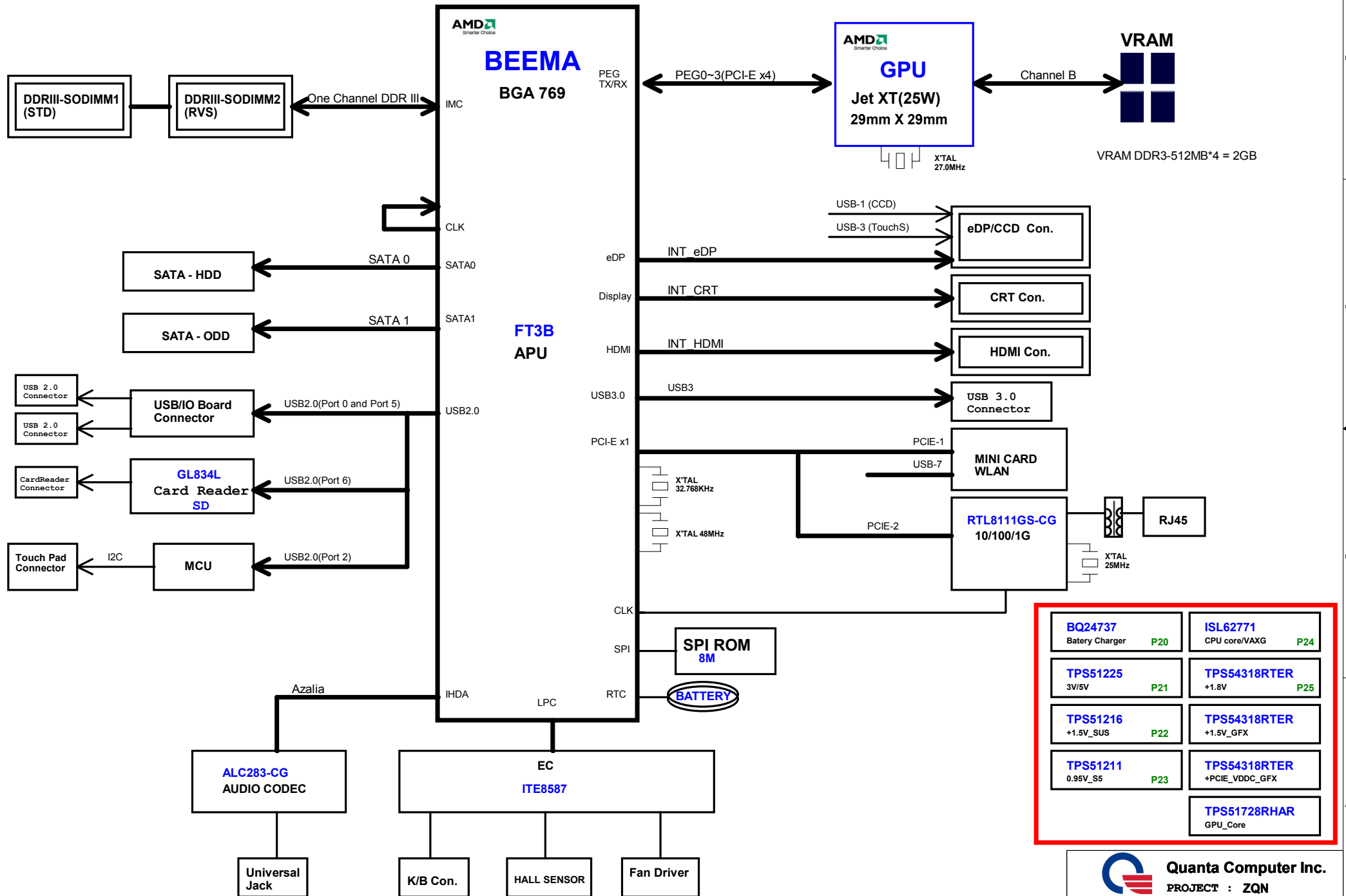


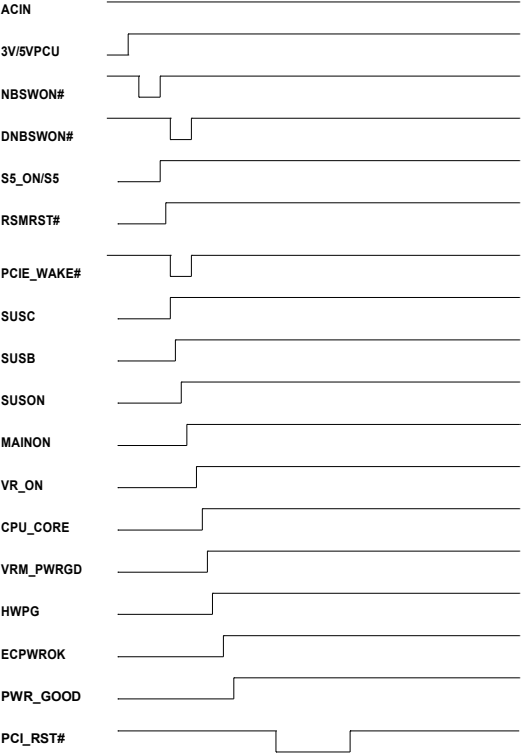
ZQN BLOCK DIAGRAM



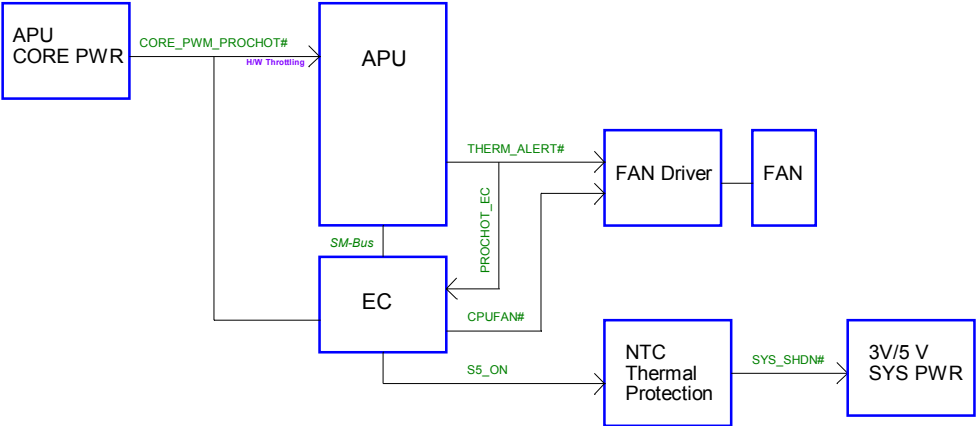
Power States

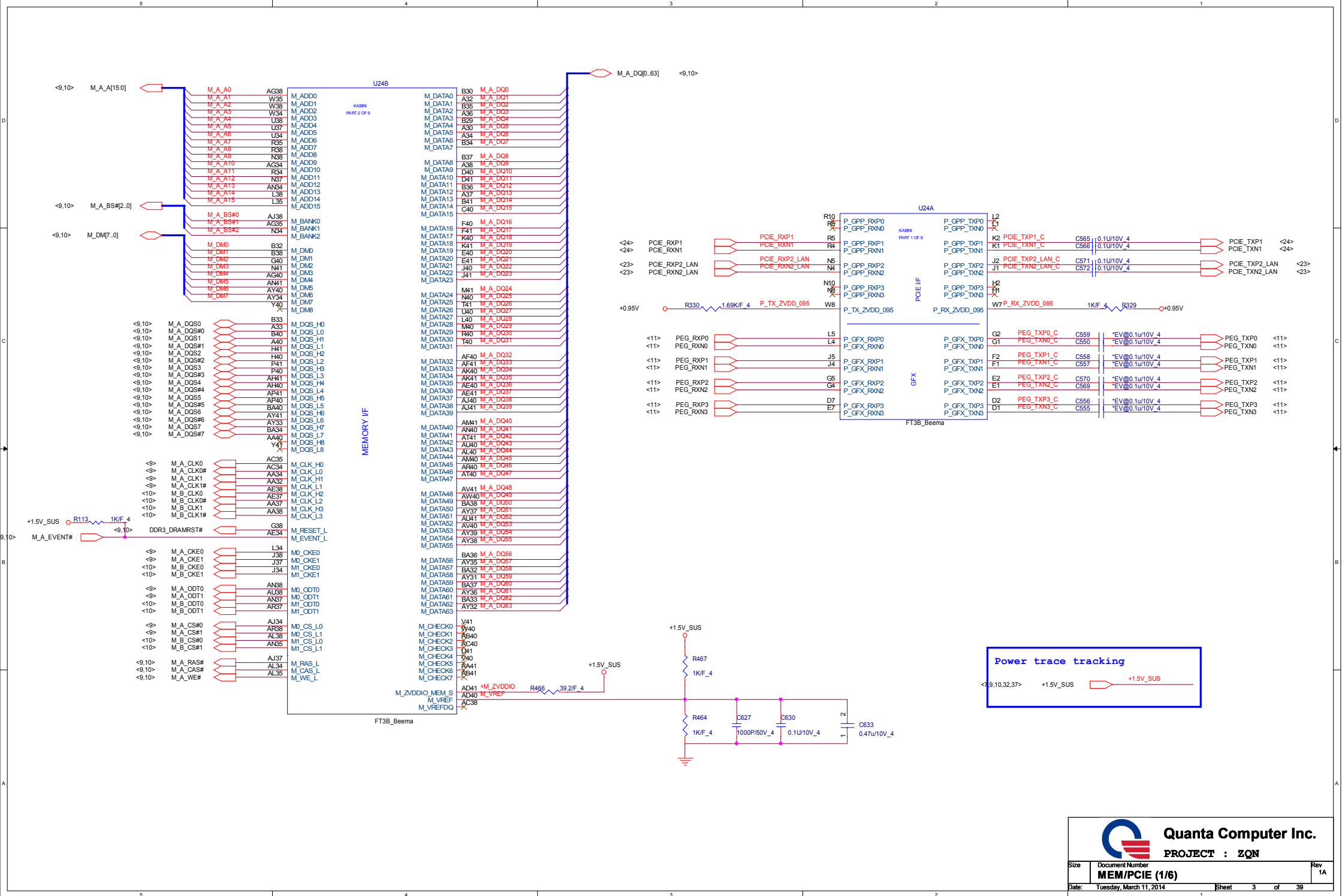
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+1.5V_RTC	+1.5V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/ TPM POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+1.8V_S5	+1.8V	APU POWER	S5_ON	S0-S5
+0.95V_S5	+0.95V	APU CORE POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	APU/Peripheral component /WLAN POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+SMDDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+1.8V	+1.8V	APU POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD	MAINON	S0
+0.95V	+0.95V	APU CORE POWER	MAINON	S0
+VDDNB_CORE	variation	APU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+VGPU_CORE	variation	GPU POWER	DGPU_PWREN	S0
+1.5V_GFX	+1.5V	GPU POWER	DGPU_PWREN	S0
+1.8V_GFX	+1.8V	GPU POWER	DGPU_PWREN	S0
+3V_GFX	+3V	GPU POWER	DGPU_PWREN	S0

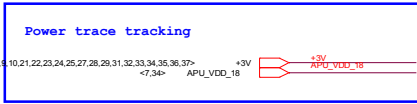
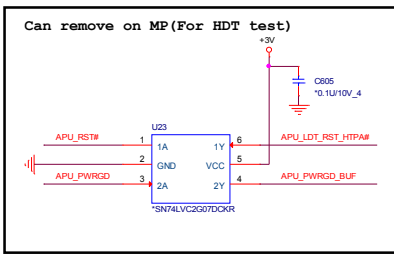
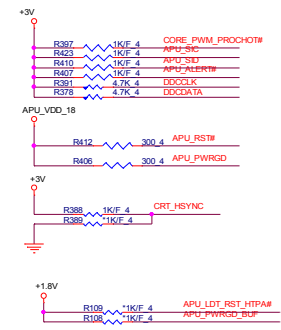
Power Sequence



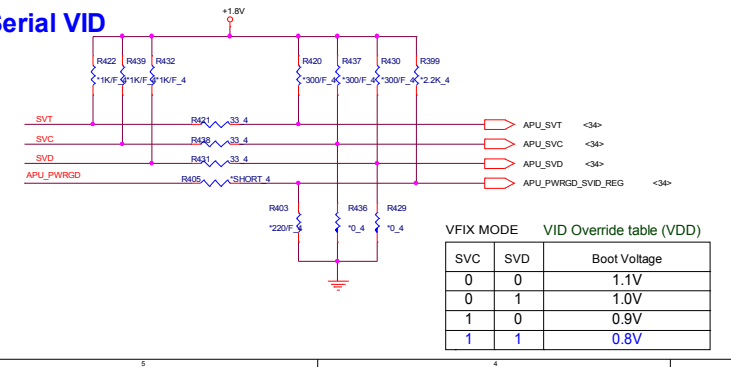
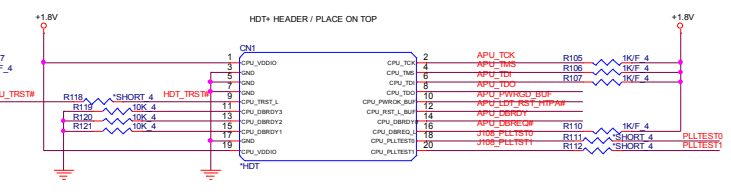
Thermal Follow Chart



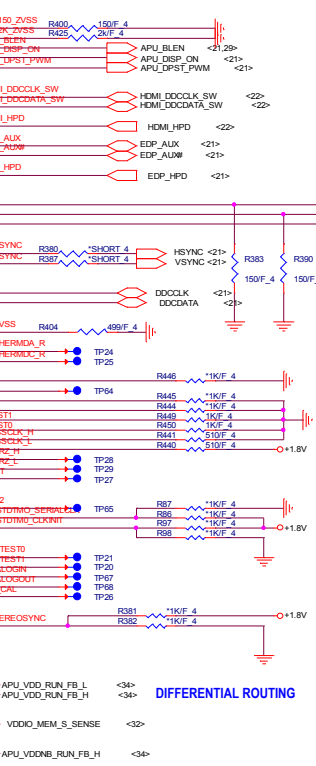
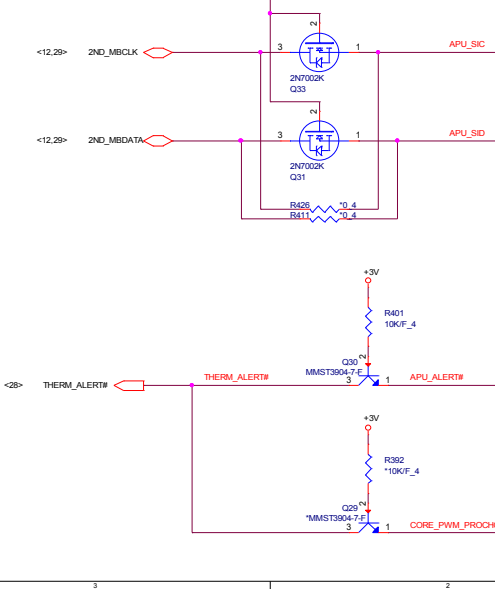




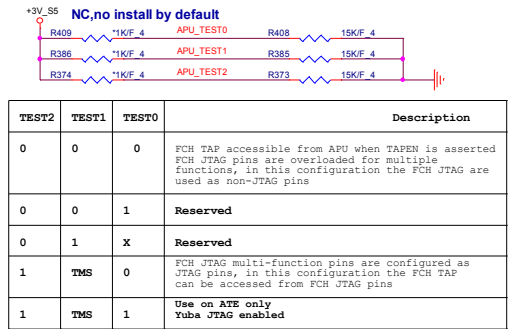
HDT(Hardware Debug Tool) Connector



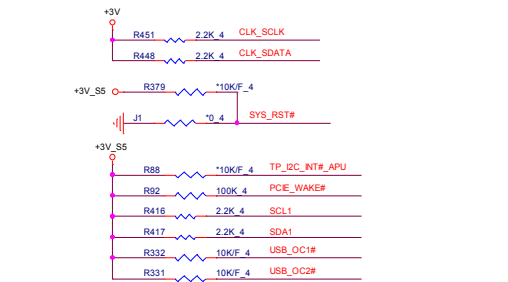
SMBUS (Internal Thermal sensor)



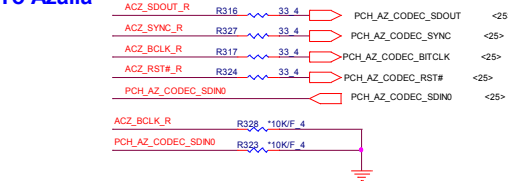
Test mode setting (Follow AMD's suggestion)



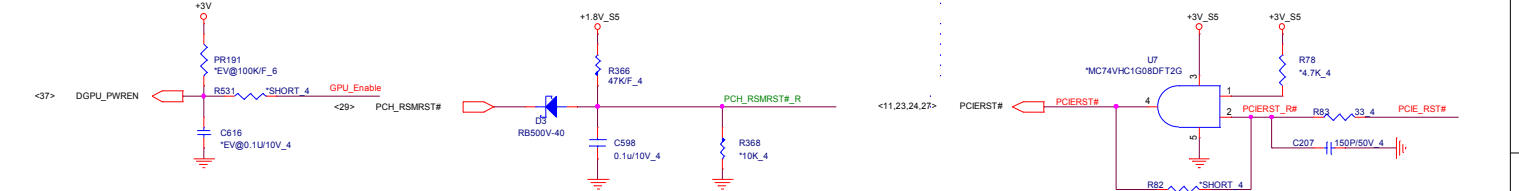
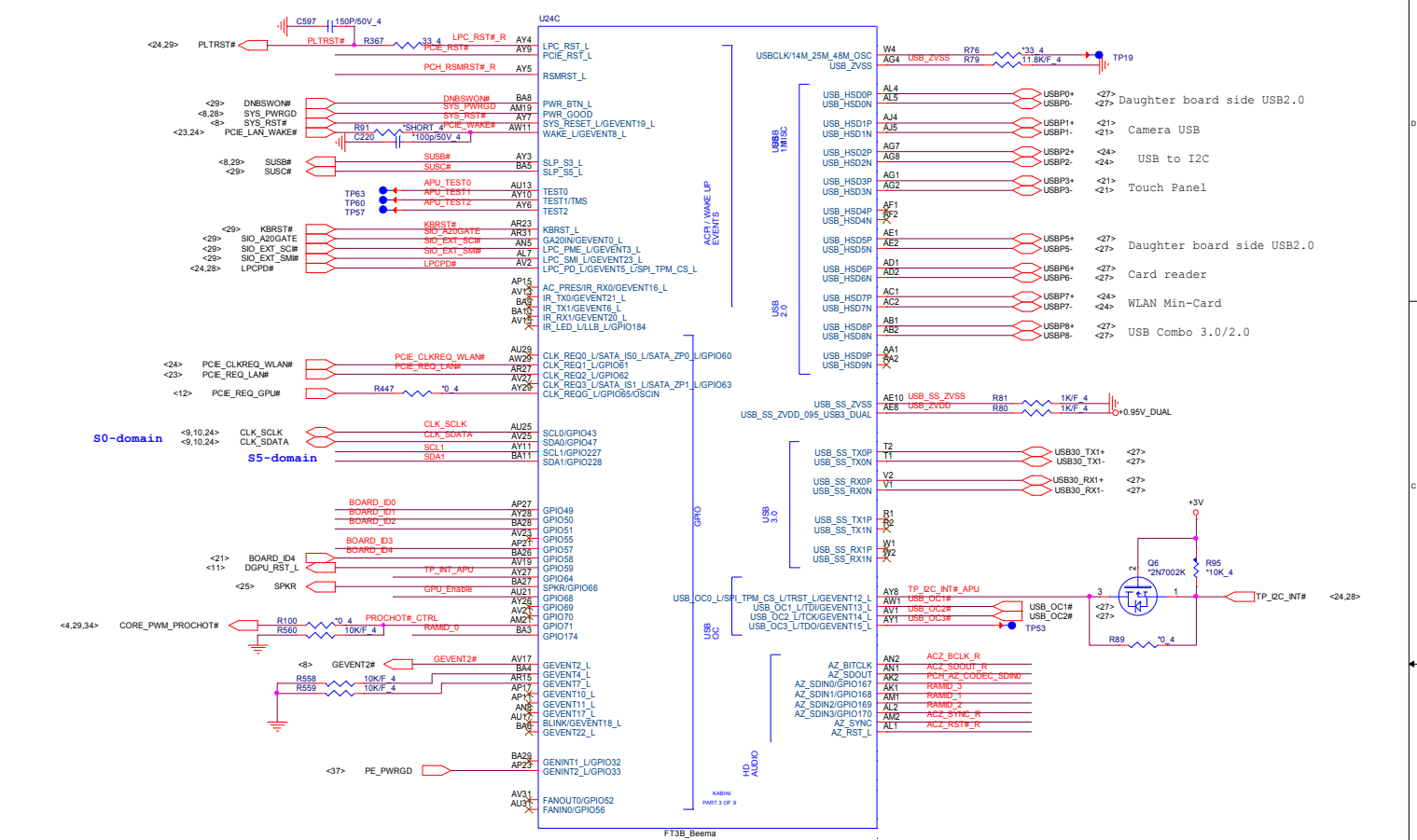
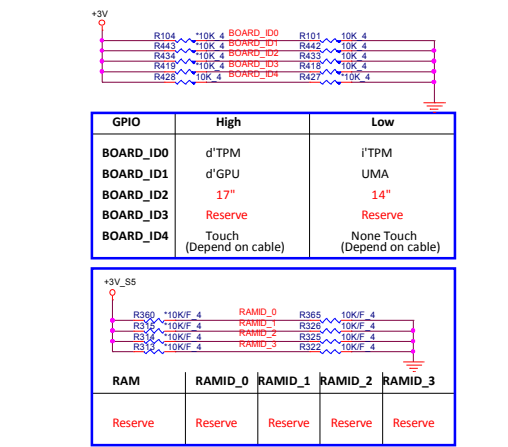
External pull-up



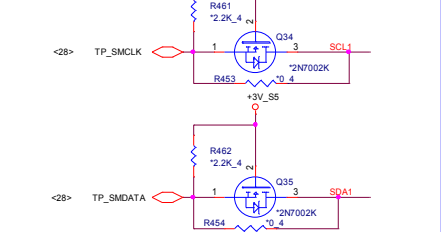
To Azalia



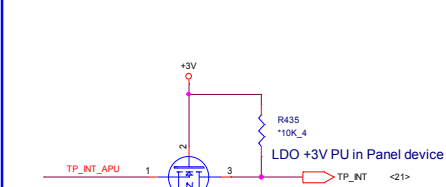
Board ID



TP SMBus



TS interrupt (reserve only)




Power trace tracking


<4.7,9.10,21,22,23,24,25,27,28,29,31,32,33,34,35,36,37>

+3V  +3V


<4.7,35>

+1.8V  +1.8V

<6.7,8,23,24,26,27,28,29,31,36>

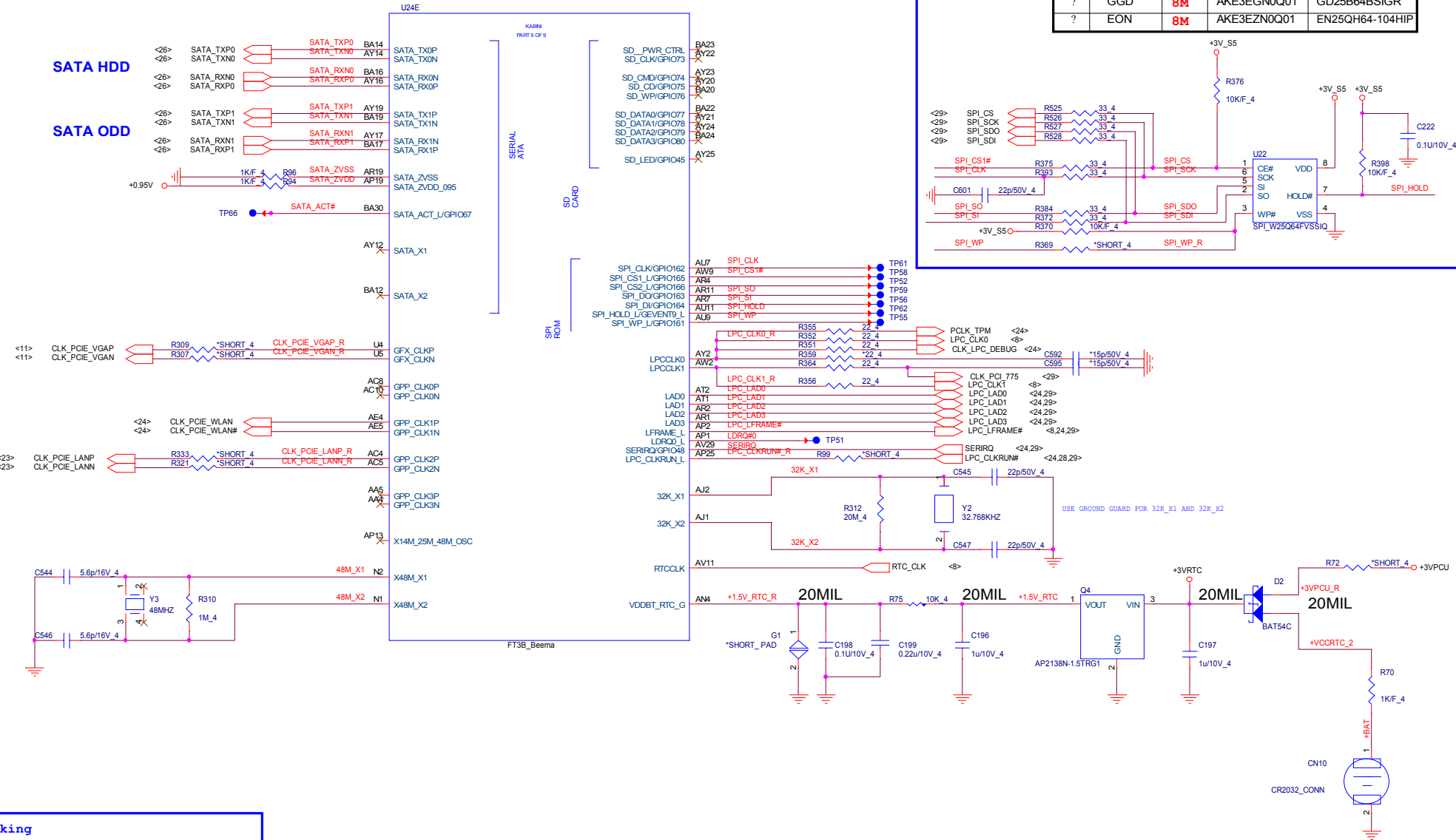
+3V_SS  +3V_SS

<7>

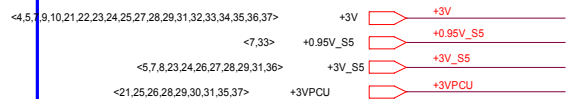
+0.95V_DUAL  +0.95V_DUAL

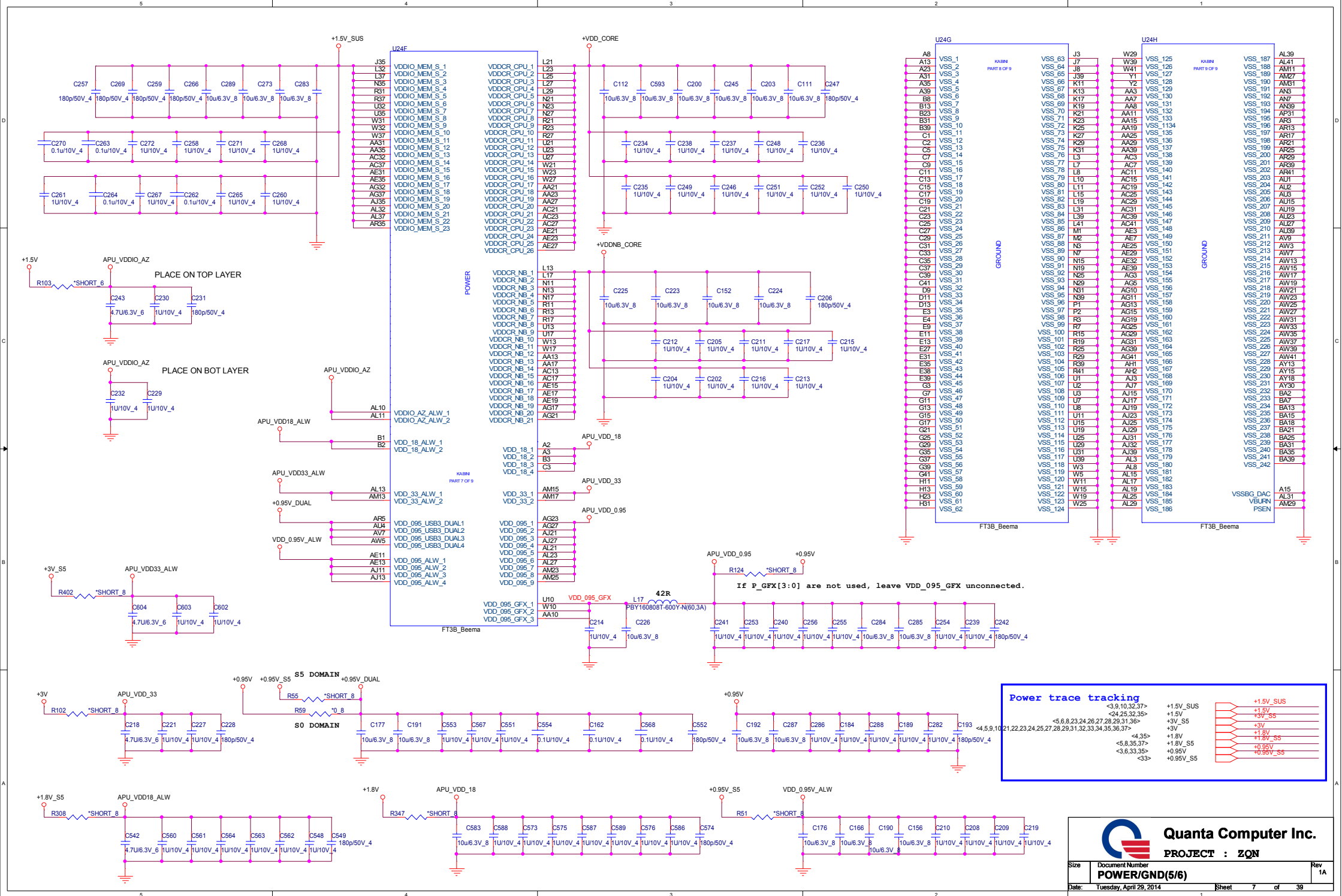
APU SPI ROM

	Vender	Size	Quanta P/N	Vender P/N
1st	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
?	AMIC	8M	?	?
?	MAX	8M	?	MX25L6436E
?	GGD	8M	AKE3EGN0Q01	GD25B64BSIGR
?	EON	8M	AKE3EZN0Q01	EN25QH64-104HIP



Power trace tracking

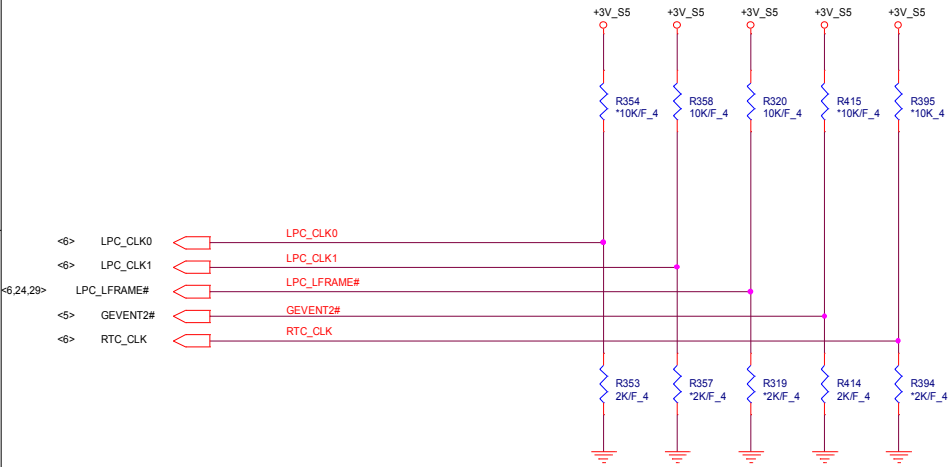




STRAPS PINS

OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

DEBUG STRAPS



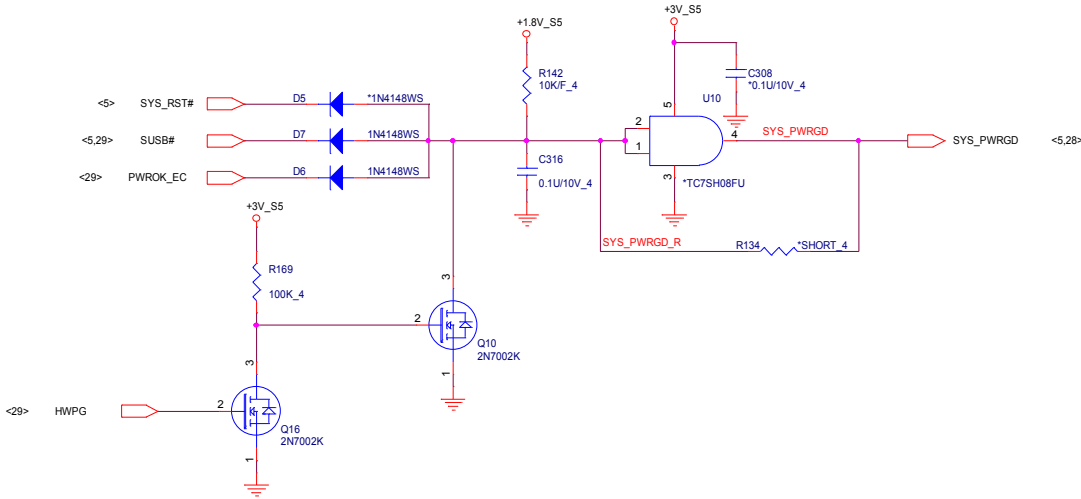
REQUIRED STRAPS

					RTC_CLK	LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH					Normal power up DEFAULT	BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW					Fast power on DEFAULT	BOOT FAIL TIMER DISABLED	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

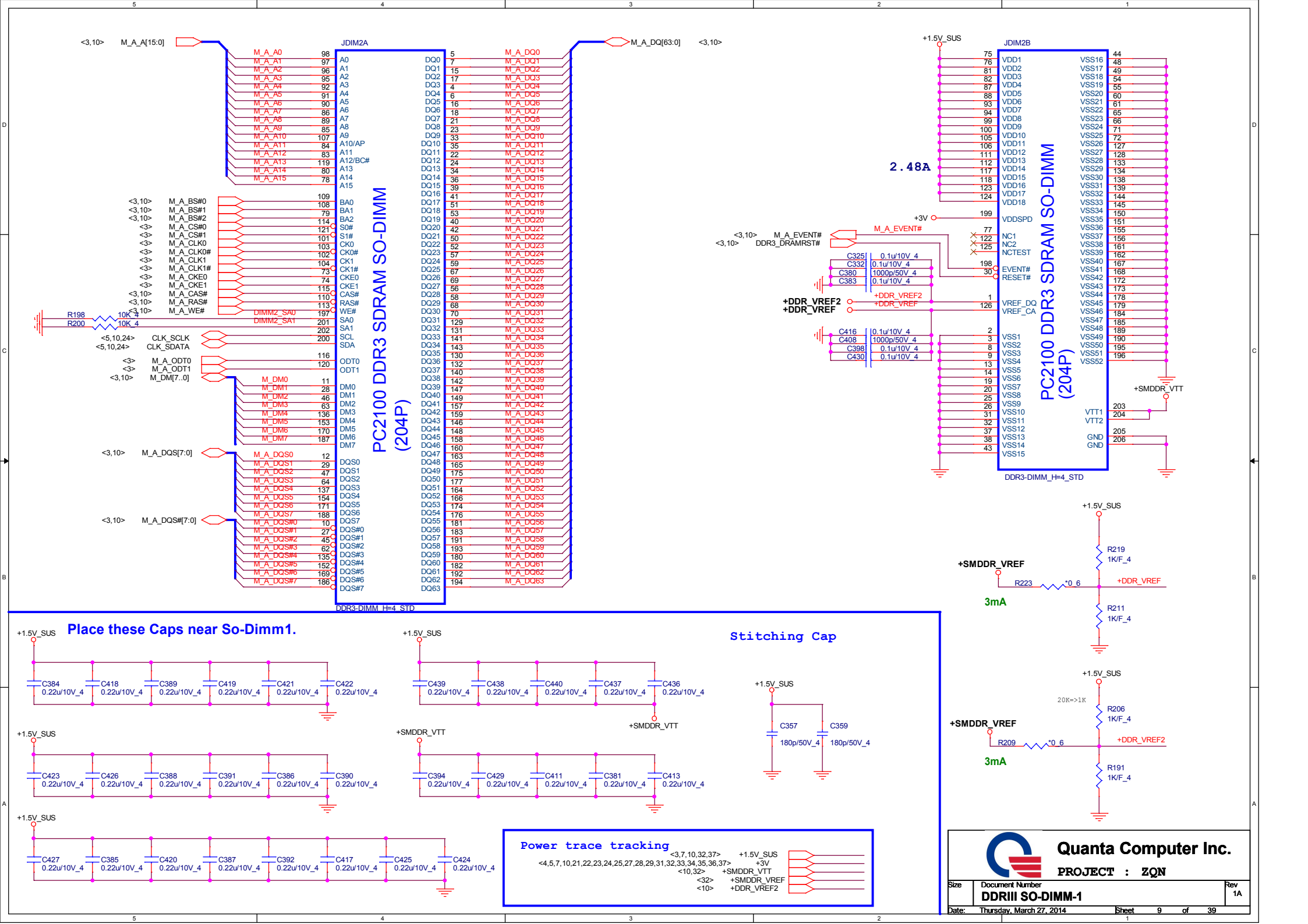
Power trace tracking

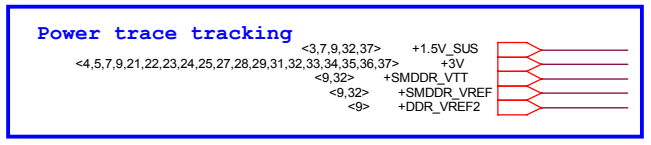
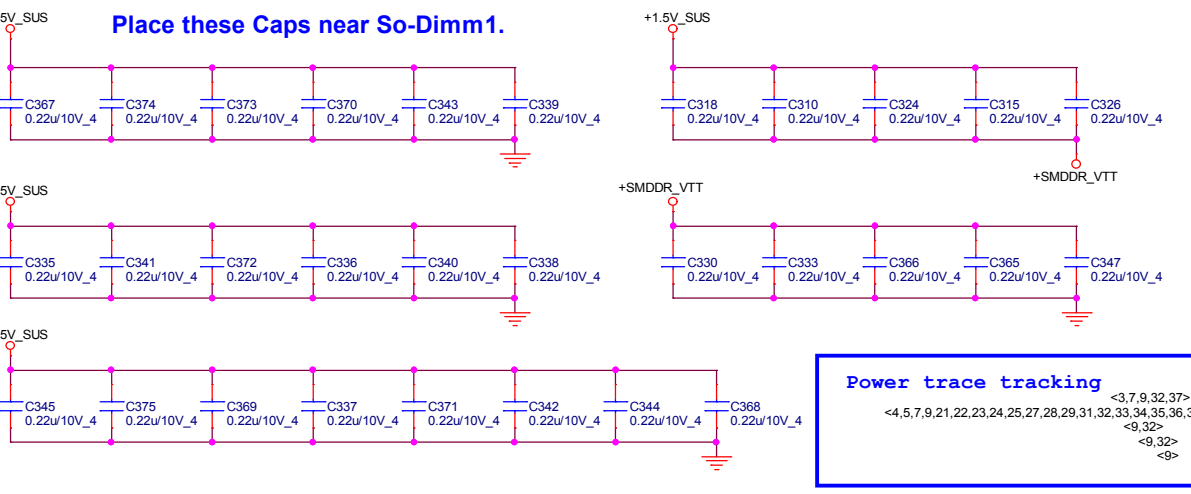
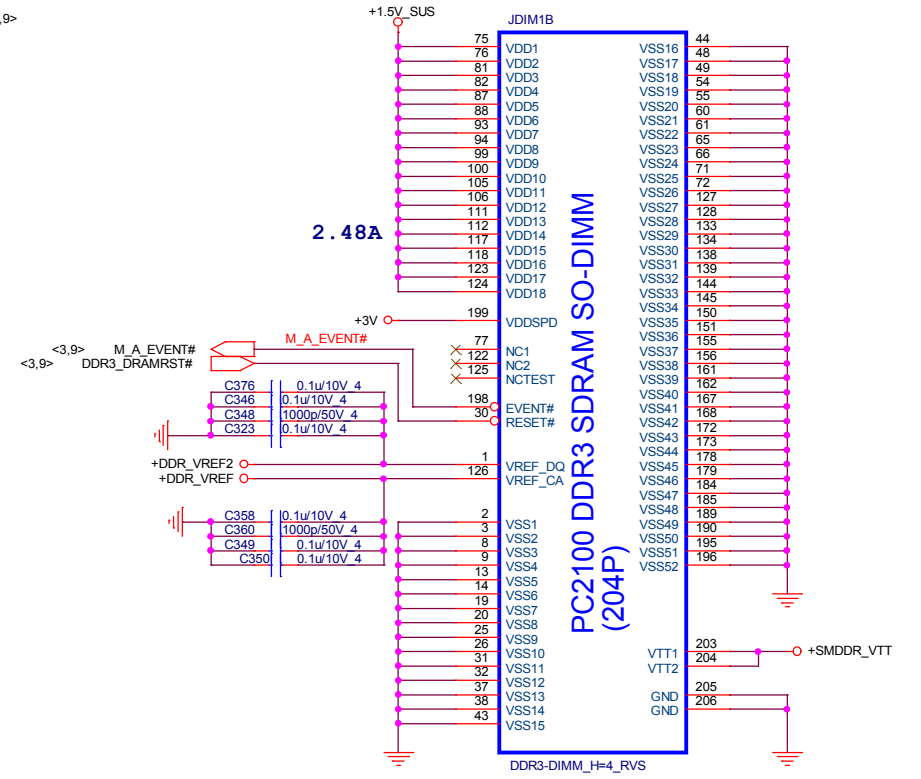
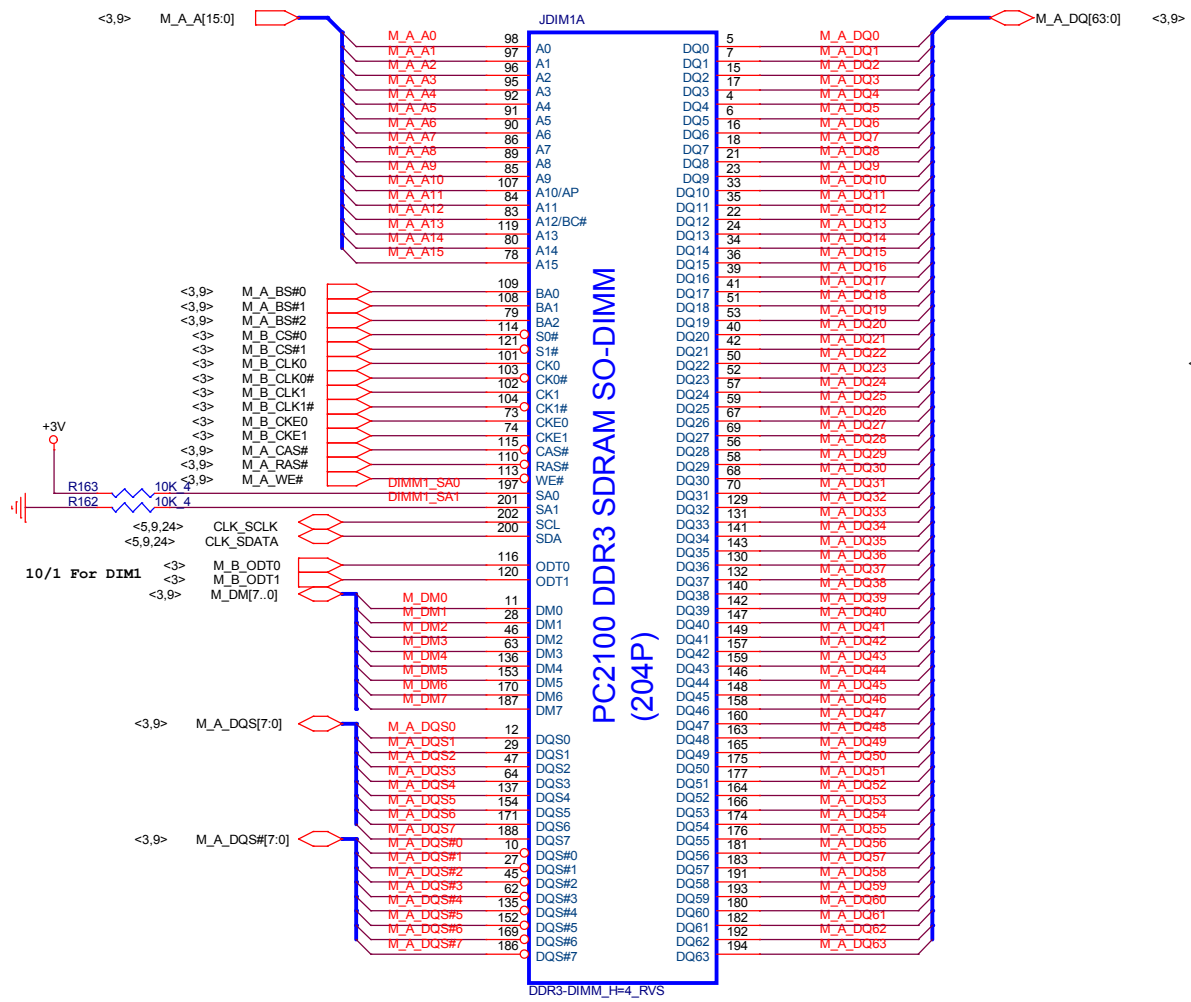


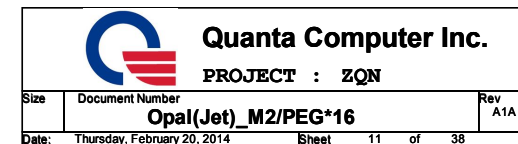
SYS_PWRGD

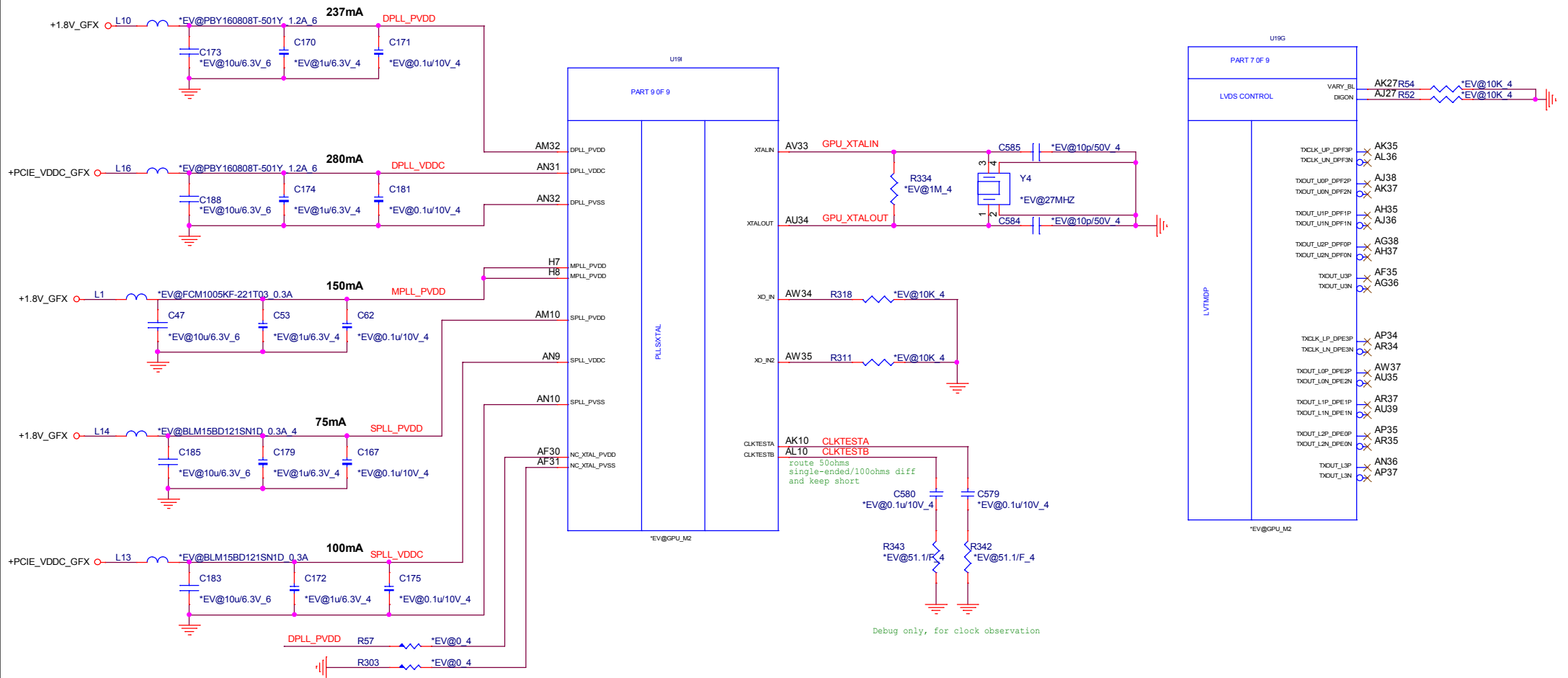


Quanta Computer Inc.
PROJECT : ZQN









Quanta Computer Inc.

PROJECT : ZQN

Size	Document Number	Rev
	Opal(Jet)_M2/ XTAL_LVDS	A1A
Date:	Thursday, February 20, 2014	Sheet 13 of 38

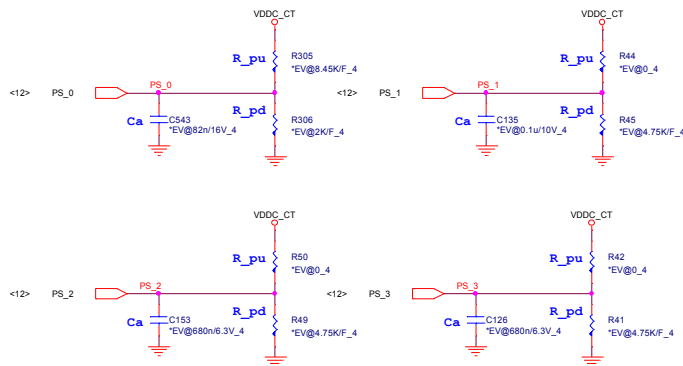
PS_3 [3:1]

Vendor	Vendor P/N	STN B/S P/N	Size	Opal	Jet
				MLPS	MLPS
Hynix	H5TC2G63FFR-11C (128Mb*16) 2Gb	AKD5MZDTW05 *4	1G		000
		AKD5MZDTW05 *8	2G	001	
	H5TC4G63AFR-11C (256Mb*16) 4Gb	AKD5PGWTW13 *4	2G		110
		AKD5PGWTW13 *8	4G		
Samsung	K4W2G1646Q-BC1A (128Mb*16) 2Gb	AKD5MGST513 *4	1G		010
		AKD5MGST513 *8	2G	011	
	K4W4G1646D-BC1A (256Mb*16) 4Gb	AKD5PGWT504 *4	2G		111
		AKD5PGWT504 *8	4G		
Micron	MT41J128M16JT-093G:K (128Mb*16) 2Gb	AKD5MGSTL25 *4	1G		100
		AKD5MGSTL25 *8	2G	101	
	MT41J256M16HA-093G:E (256Mb*16) 4Gb	AKD5PZSTL02 *4	2G		
		AKD5PZSTL02 *8	4G		

System Memory Aperture size

GPIO9		GPIO11	GPIO12	GPIO13
BIOSROM		ROMIDCFG0	ROMIDCFG1	ROMIDCFG2
0	128M	0	0	0
0	256M	1	0	0
0	64M	0	1	0
0	Reservd	1	1	0

CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select if GPIO22 = 0, defines memory aperture size if GPIO22 = 1, defines ROM type 100 - 512kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 110 - 2Mbit M25P20 (ST) 111 - 4Mbit M25P40 (ST) 101 - 8kbit M25P80 (ST) 100 - 512kbit Pm25LV612 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	xxx
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	xx
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	xxx



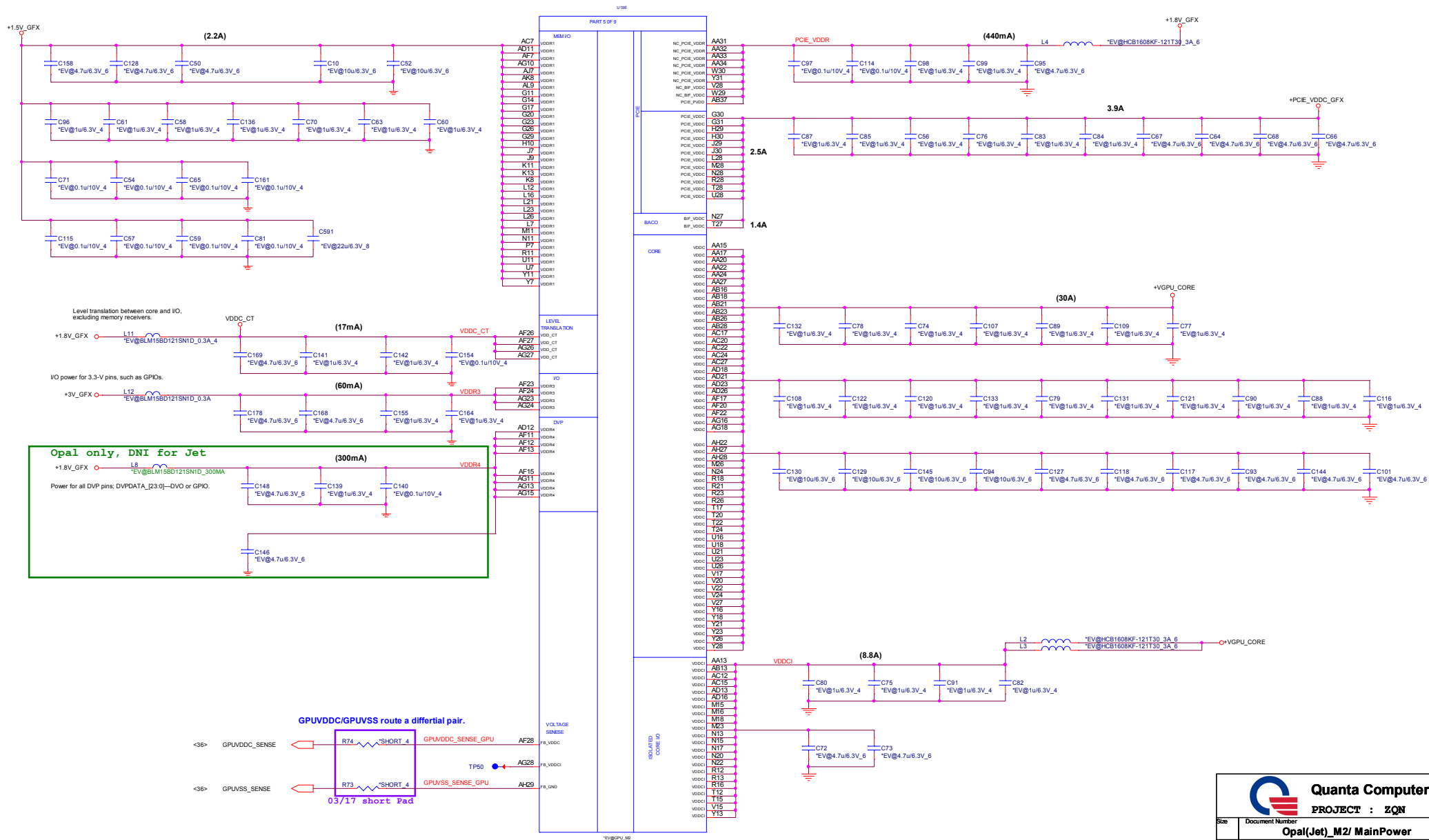
MLPS

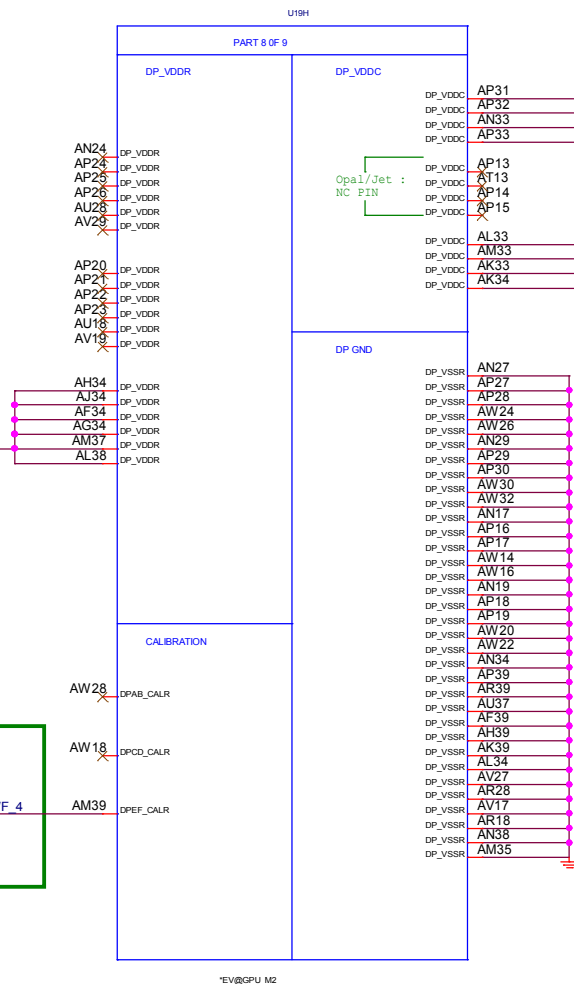
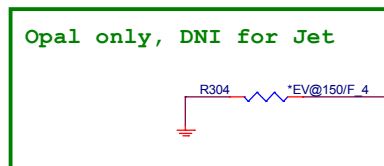
R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	10K	110
4.75K	NC	111

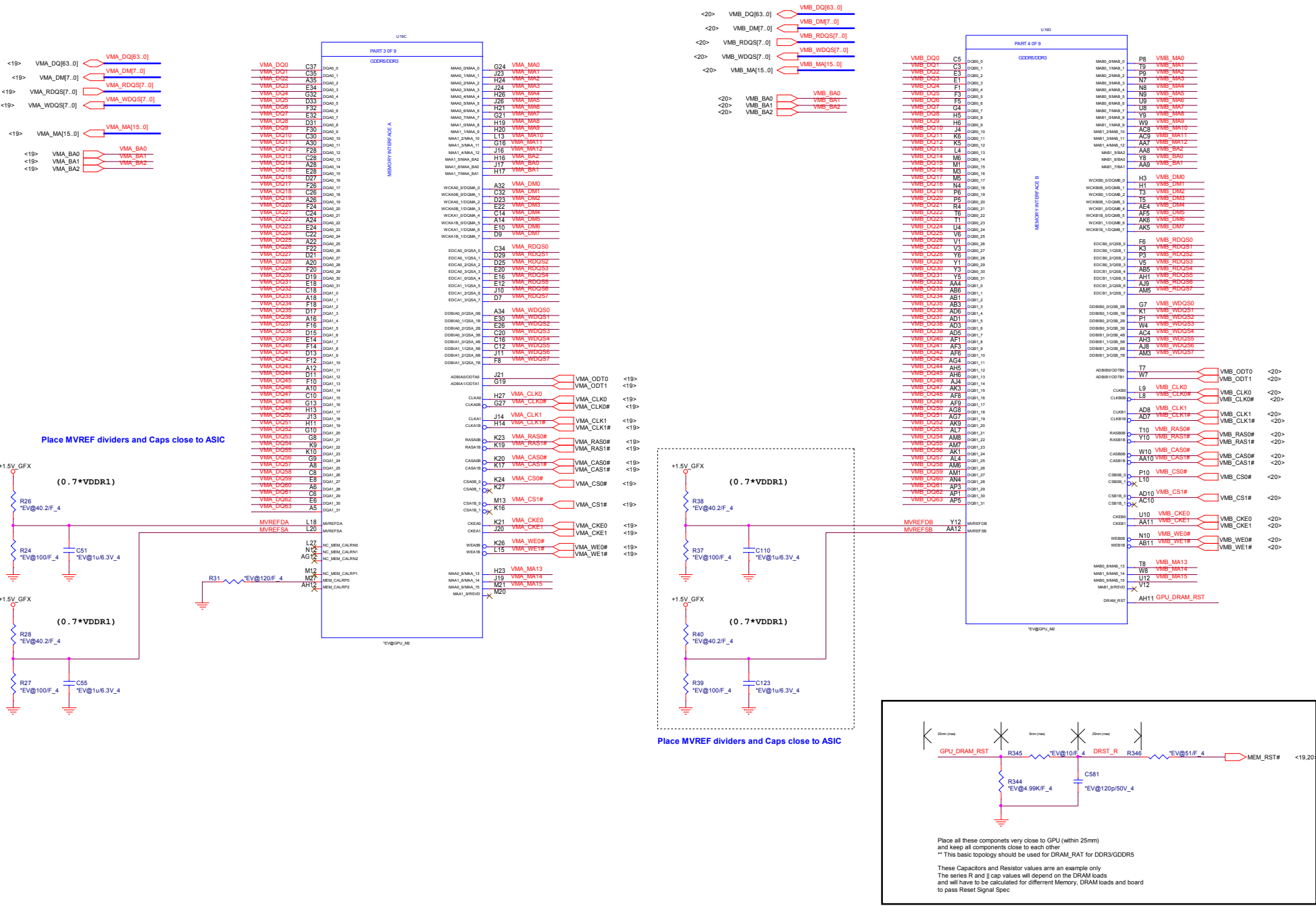
Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
10K	CS31002FB26

MLPS Bit	Bits [5:1]
PS_0	01001
PS_1	11000
PS_2	00000
PS_3	00XXX

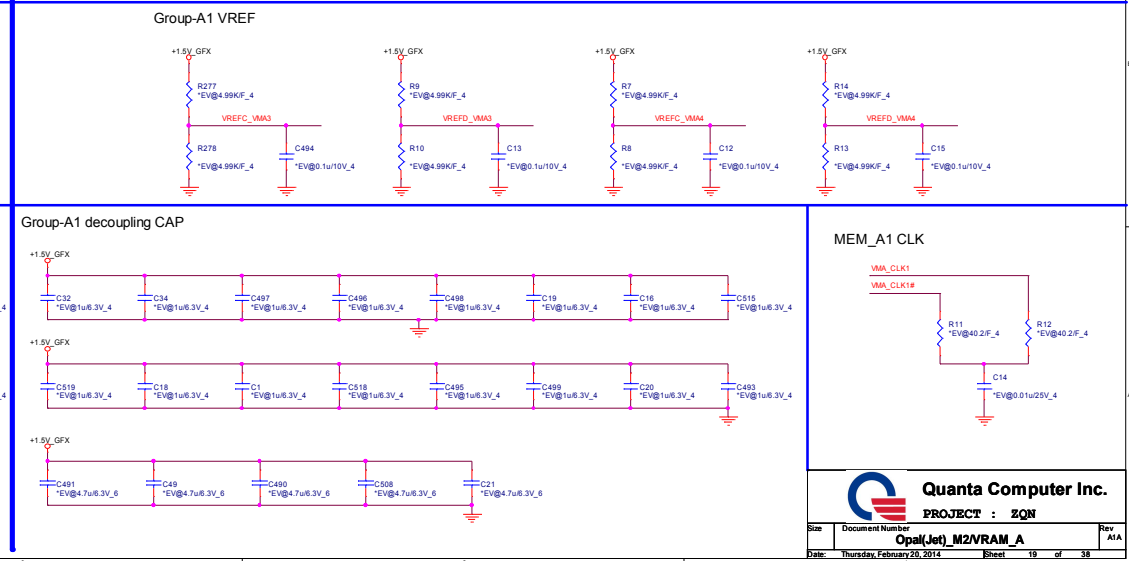
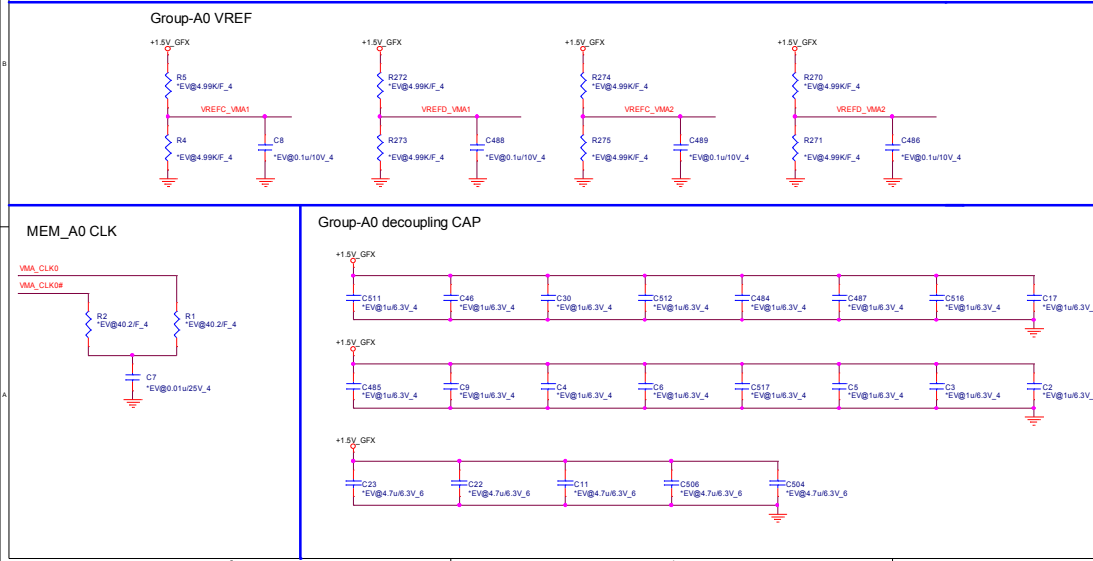
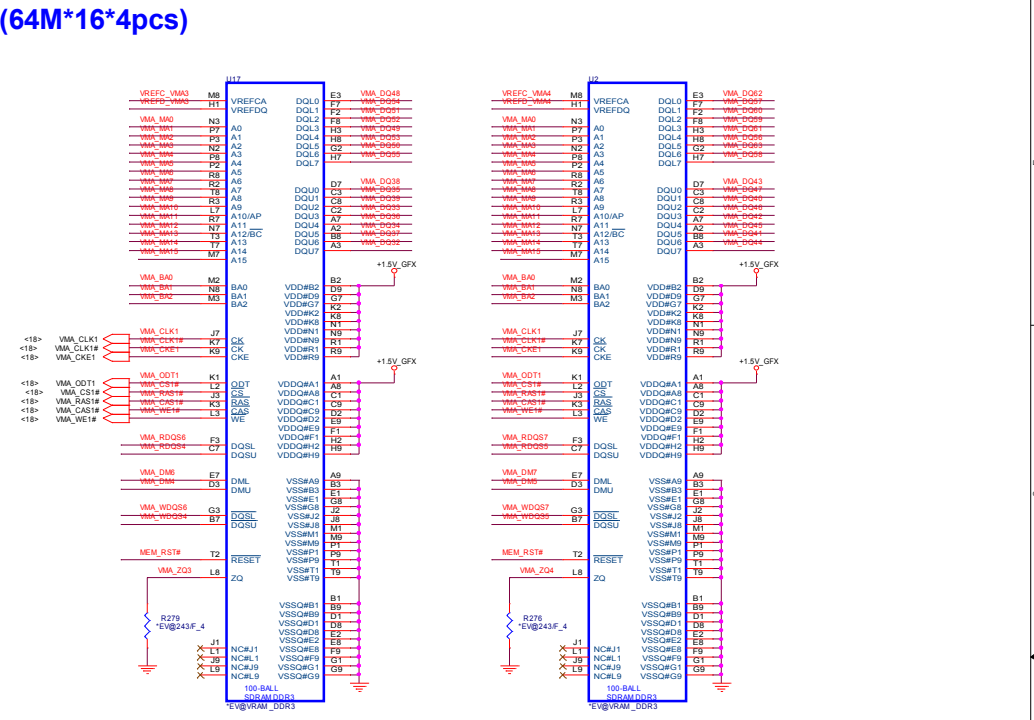
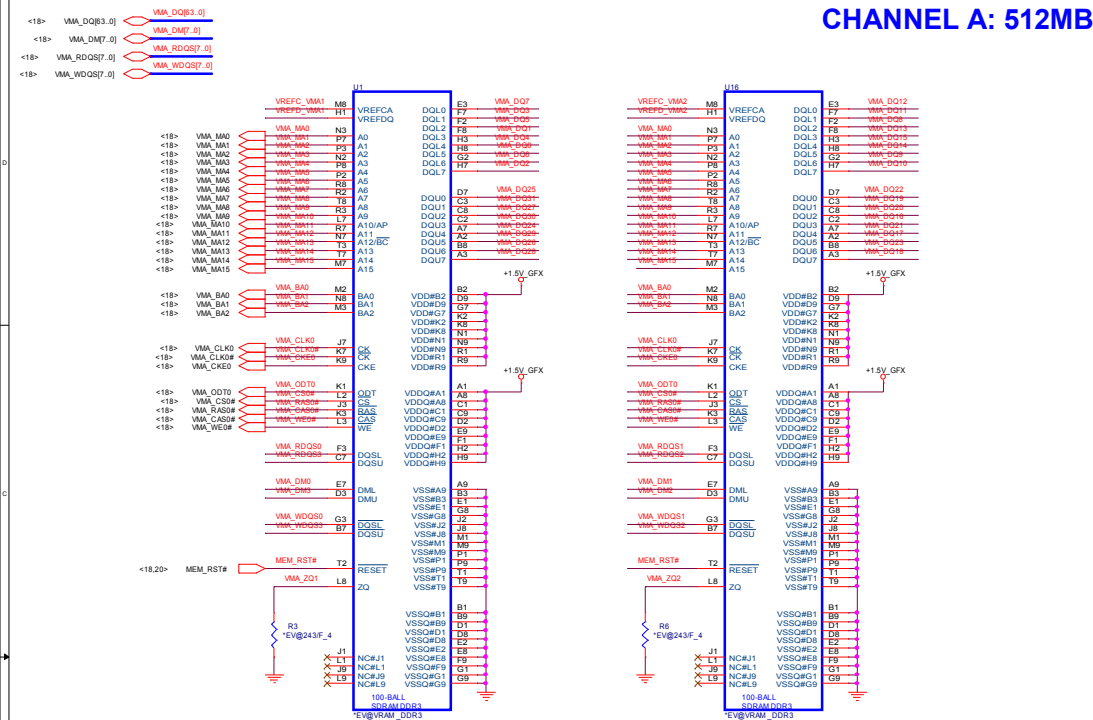
Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	



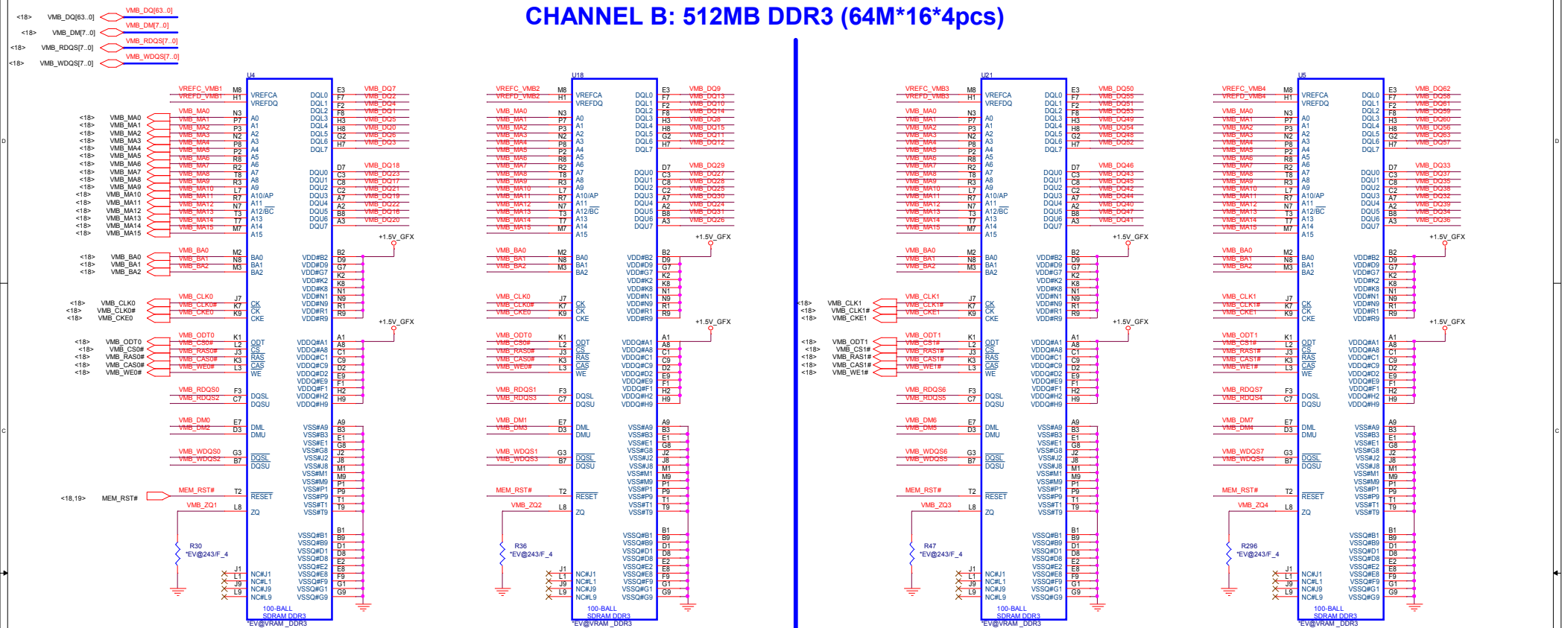




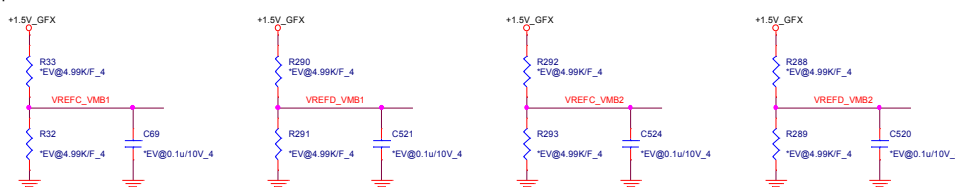
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



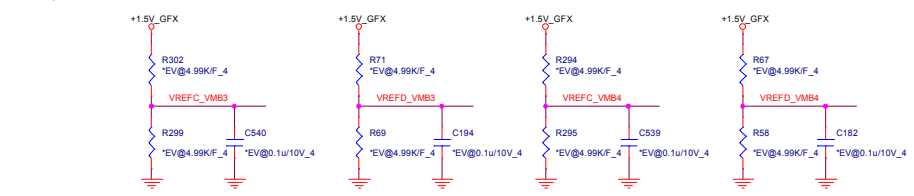
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



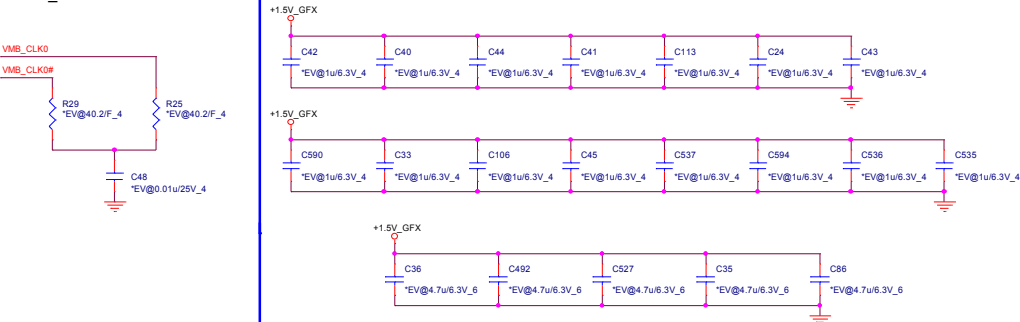
Group-B0 VREF



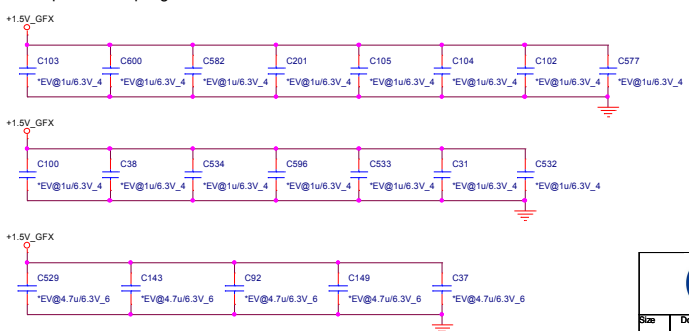
Group-B1 VREF



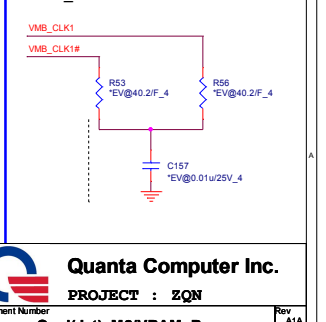
MEM B0 CLK



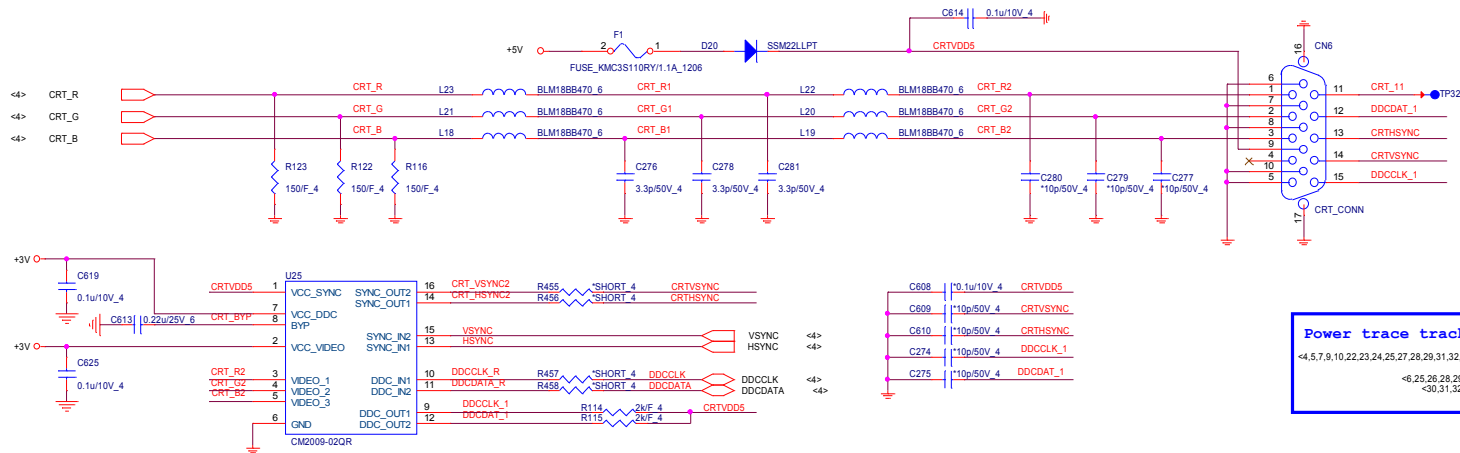
Group-B1 decoupling CAP



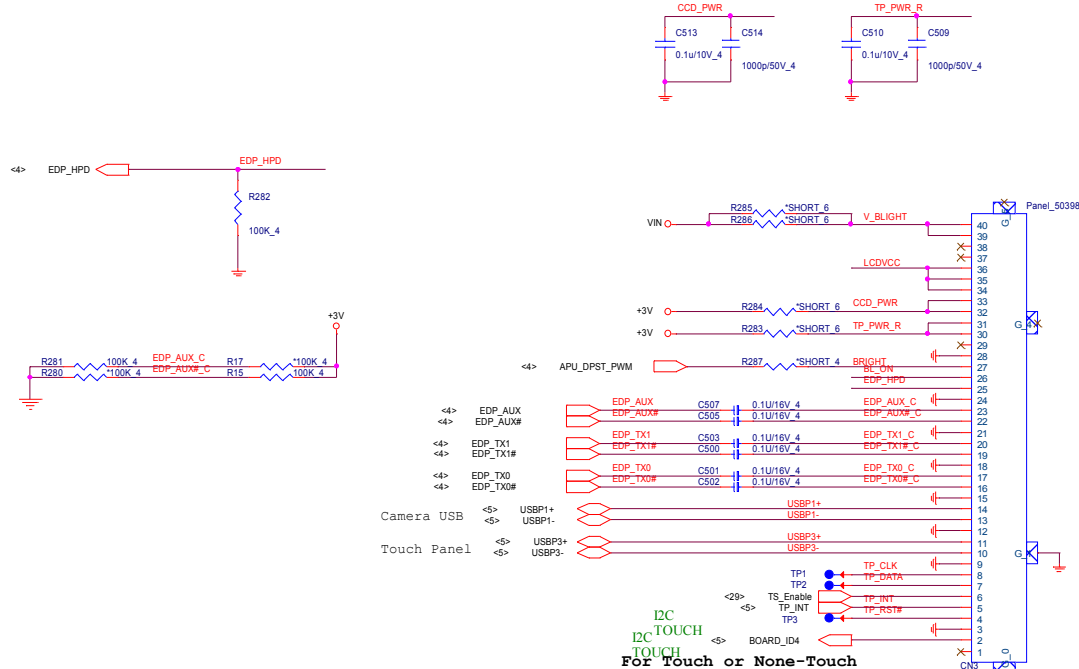
MEM B1 CLK



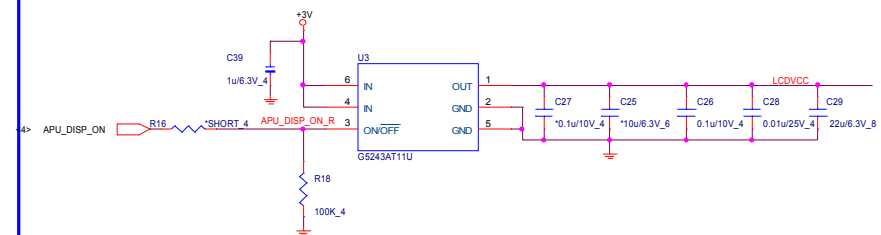
CRT



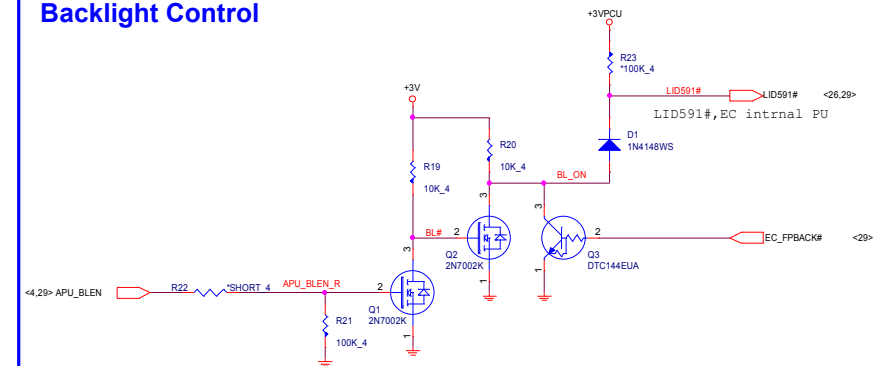
LCD CONNECTOR



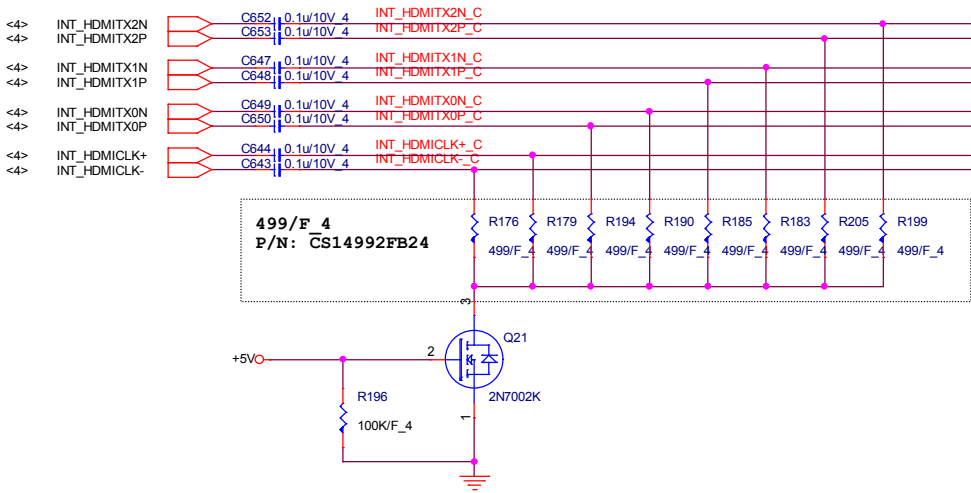
LCD Power



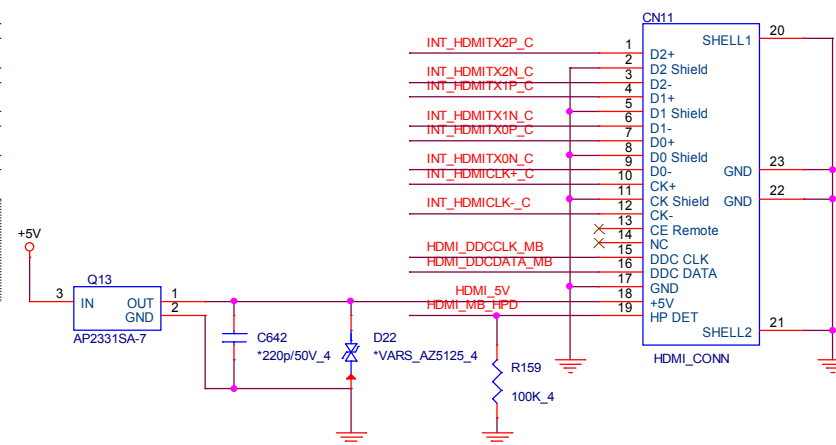
Backlight Control



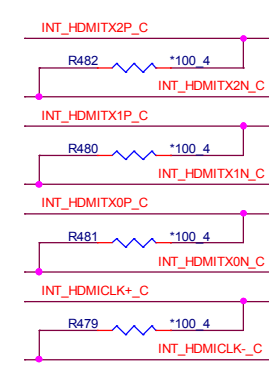
HDMI



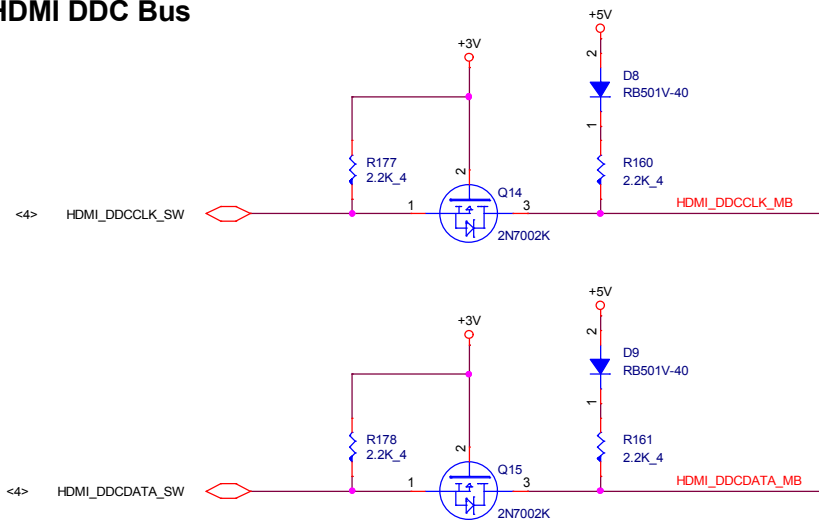
HDMI connector



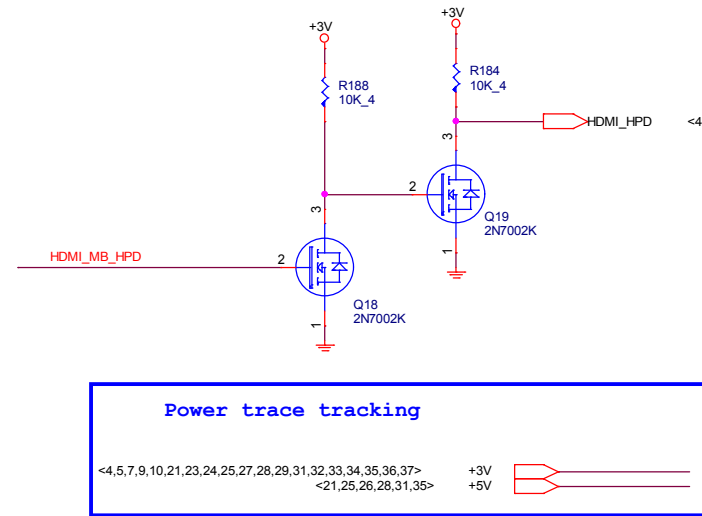
EMI



HDMI DDC Bus



HDMI-detect



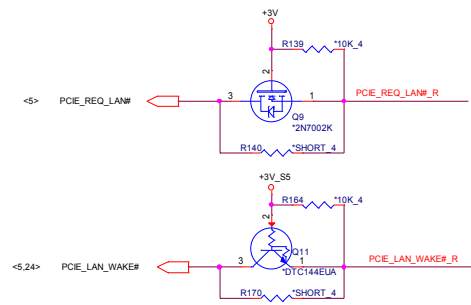
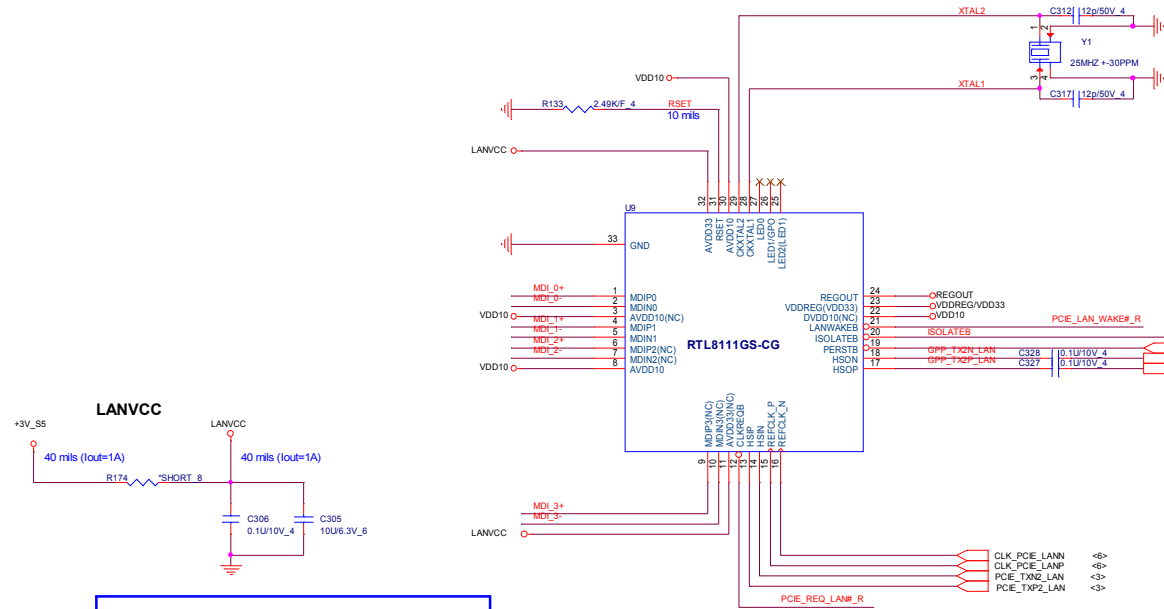
Quanta Computer Inc.

PROJECT : ZQN

HDMI (PS8101)

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LAN

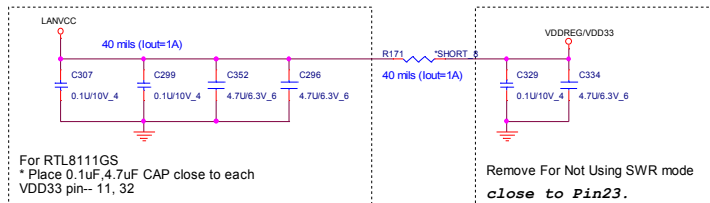


Consider VCC33 may be connected to Main Power or chipselect/bios's GPO, the pull-down resistor R14 can be NC only when Main Power or chipselect/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S1-S5.

If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S1-S5, the pull-down resistor R14 is needed to make sure the LAN chip is well isolated.

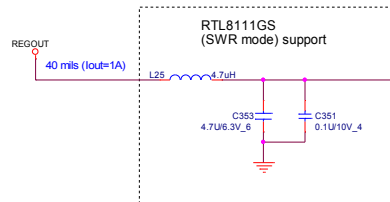
Power trace tracking

<4,5,7,9,10,22,24,25,27,28,29,31,32,33,34,35,36,37> +3V_S5 +3V

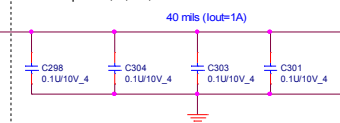


For RTL8111GS
* Place 0.1uF, 4.7uF CAP close to each VDD33 pin-- 11, 32

Remove For Not Using SWR mode
close to Pin23.



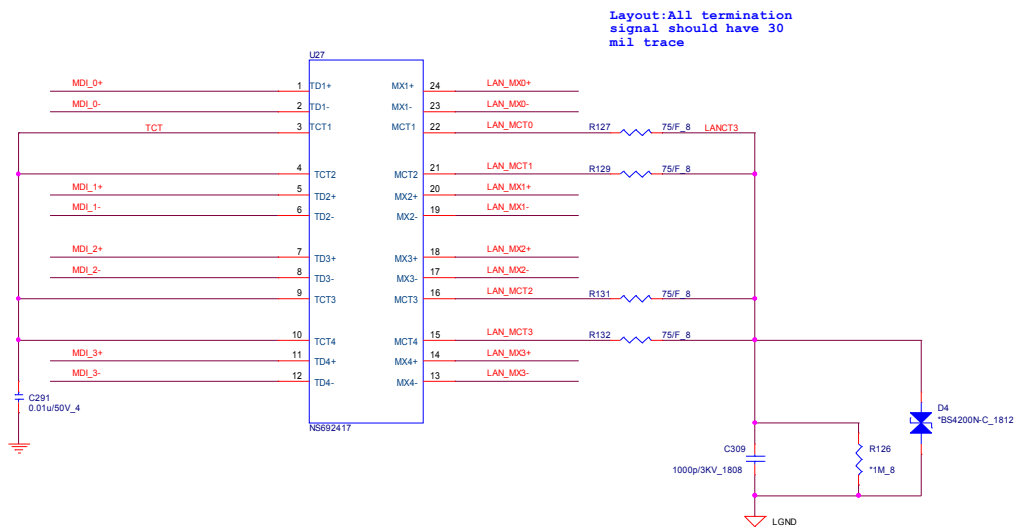
For RTL8111G(S)
* Place 0.1uF CAP close to each VDD10 pin-- 3, 8, 22, 30



For RTL8111G(S)
* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)



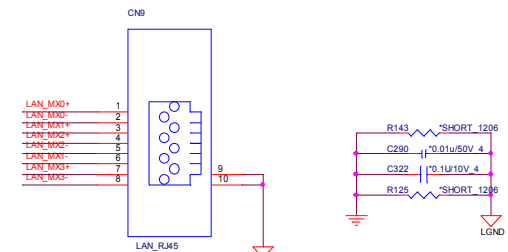
Transformer



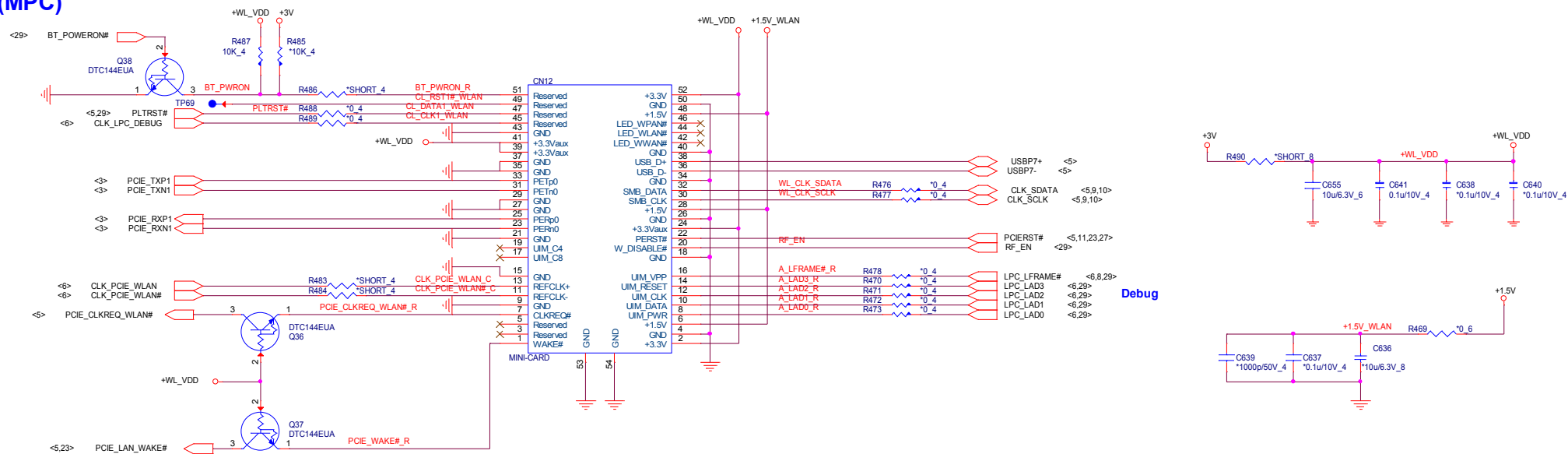
Layout: All termination signal should have 30 mil trace

RJ45 Connector

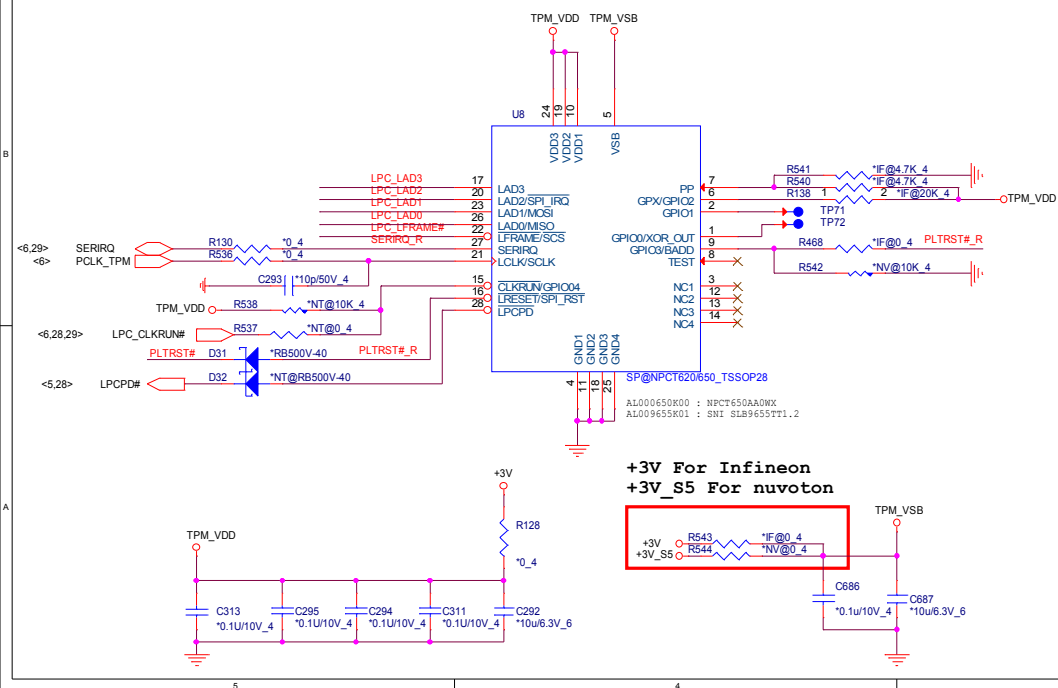
Need Check P/N and F/P



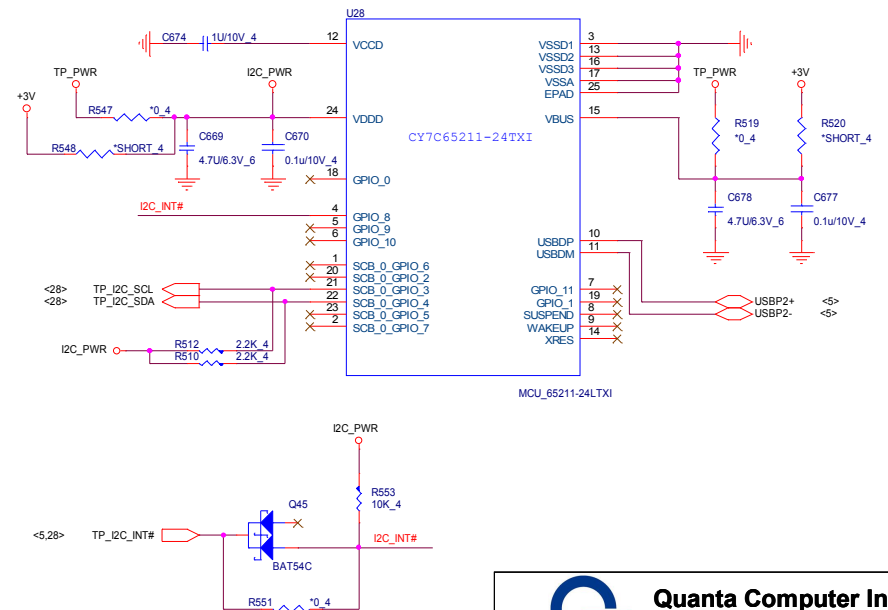
Mini Card 1 (MPC)



TPM 2/18 Check DNS parts and power source(+3V or +3V_S5)

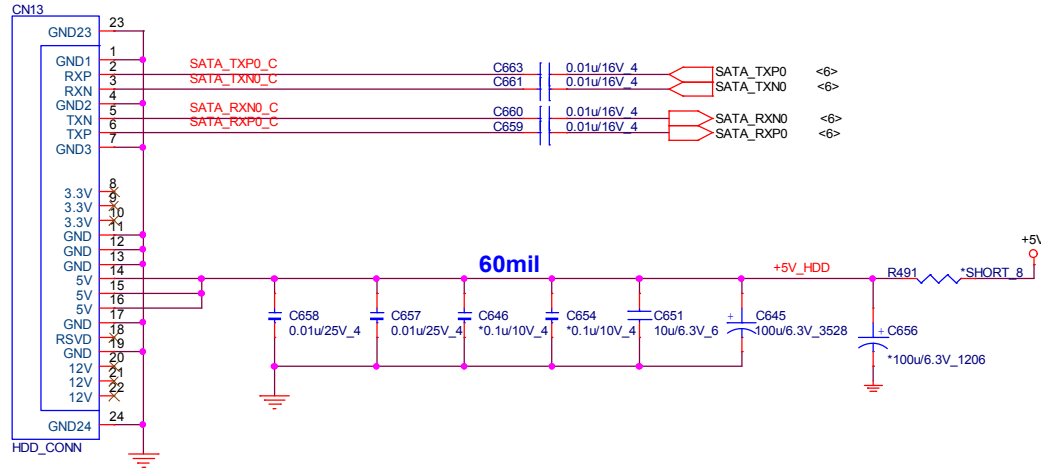


USB2I2C

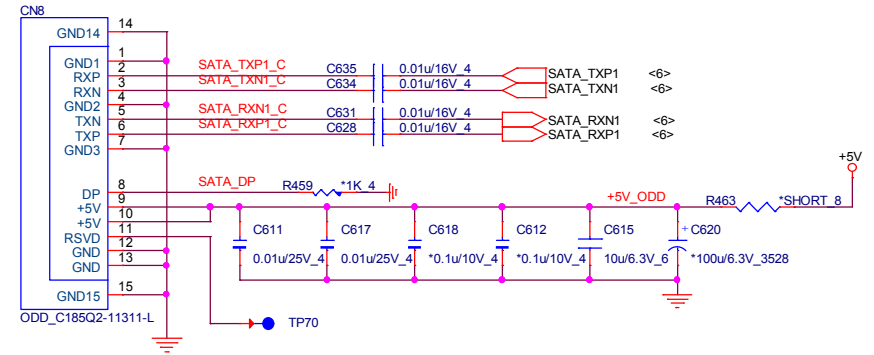


2.5" SATA HDD

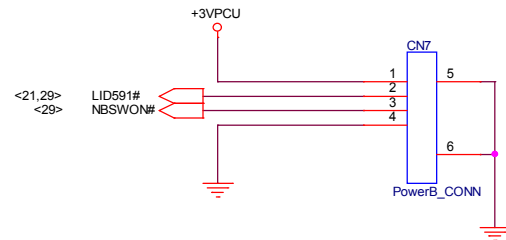
Need Check P/N and F/P



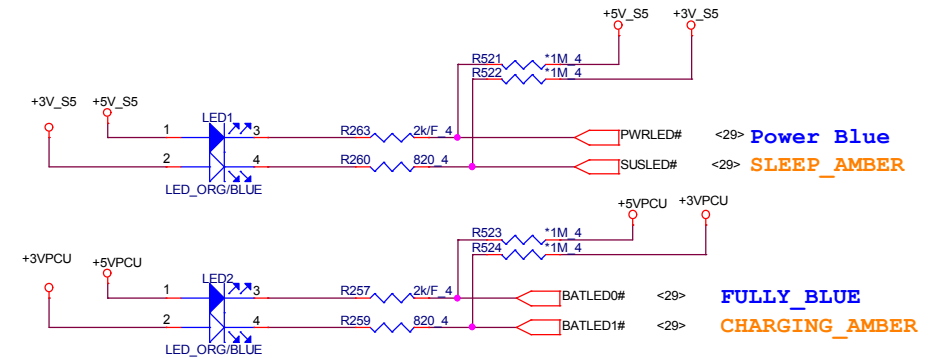
SATA ODD



Power Switch Board.



Indicitor LED



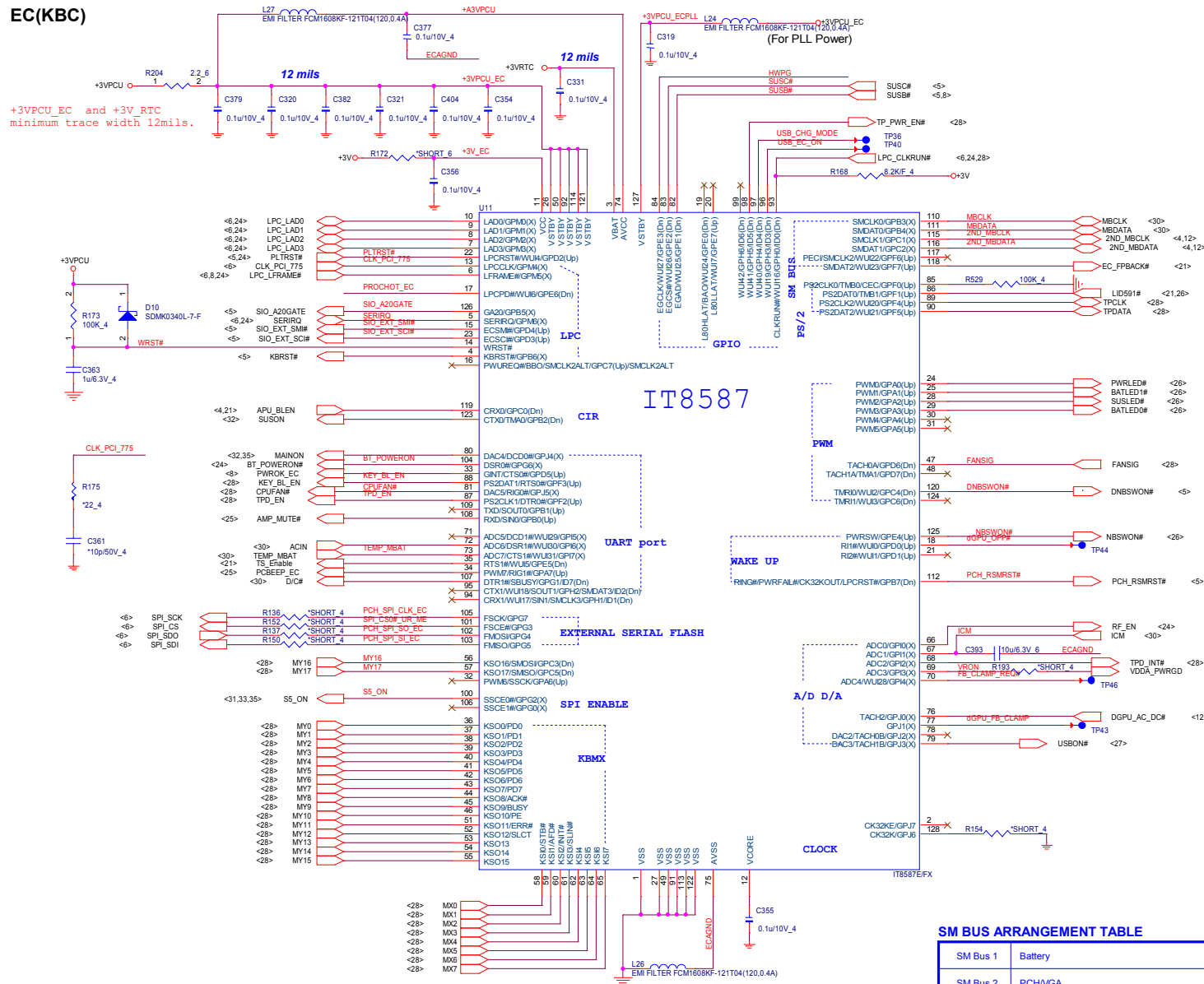
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PROJECT : ZQN

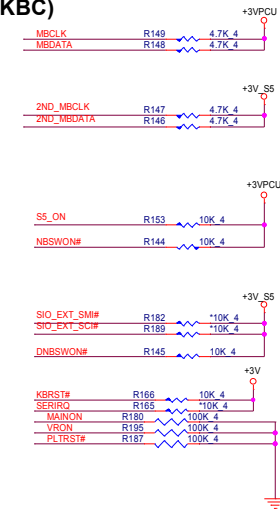
Size	Document Number	Rev
	SATA HDD/LED/SW	1A

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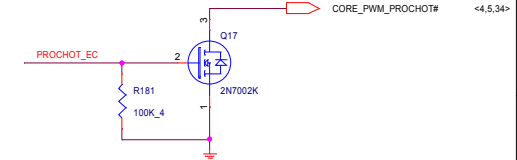
EC(KBC)



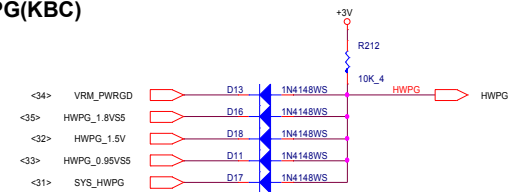
External PU(KBC)



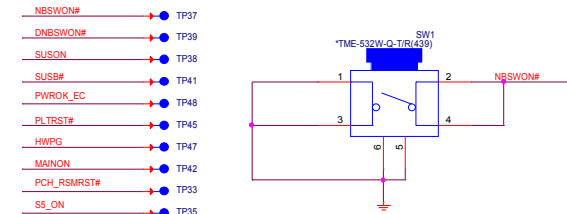
ProcHOT



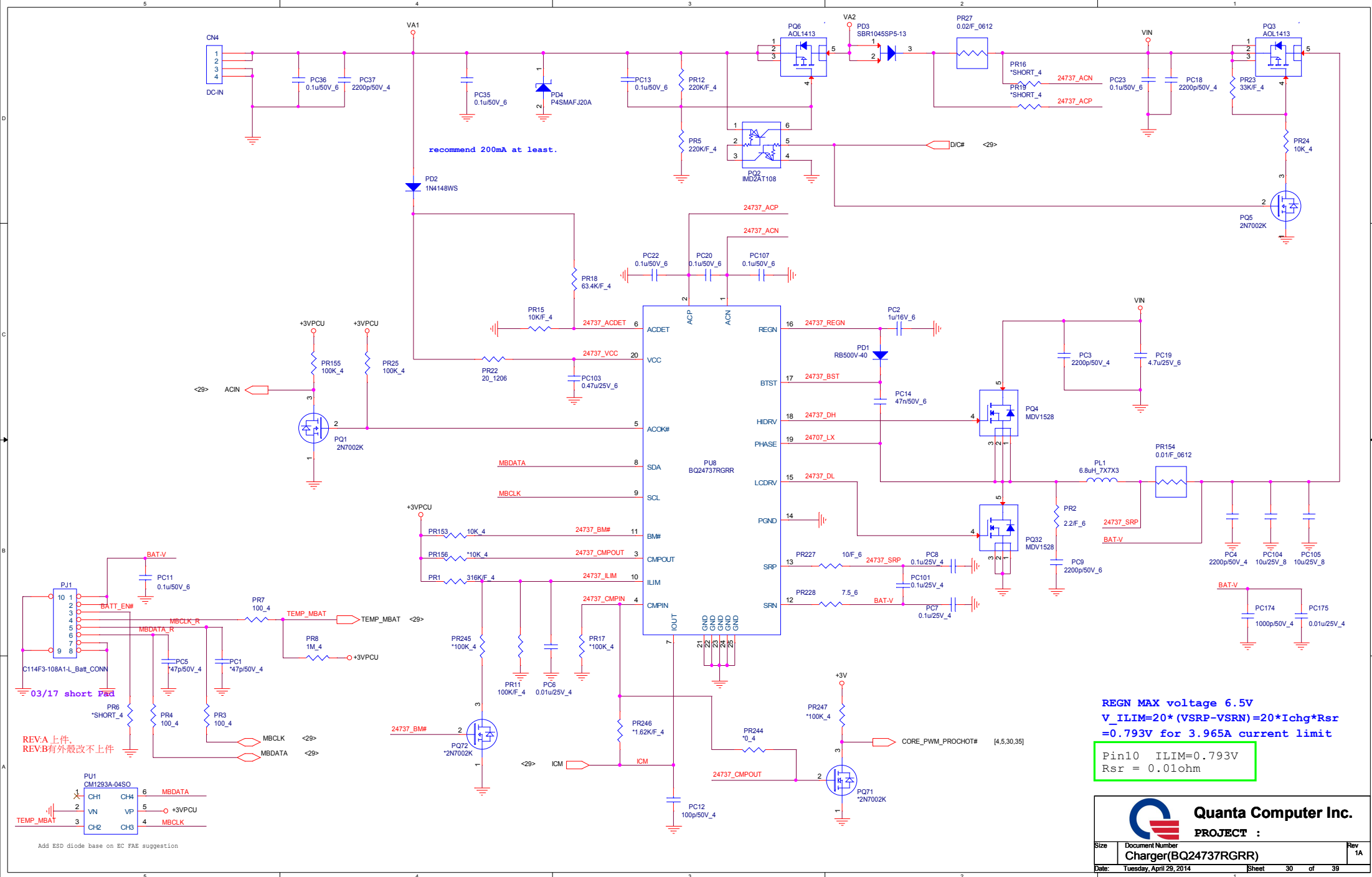
HWPG(KBC)

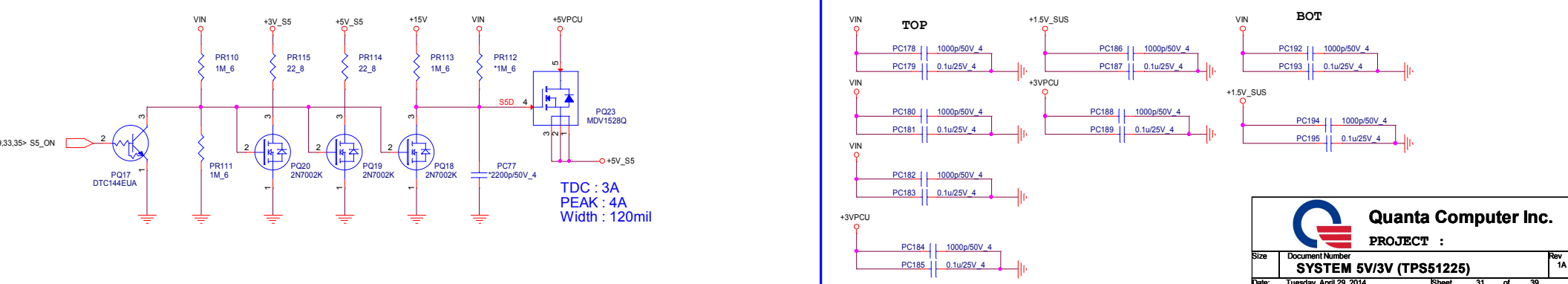
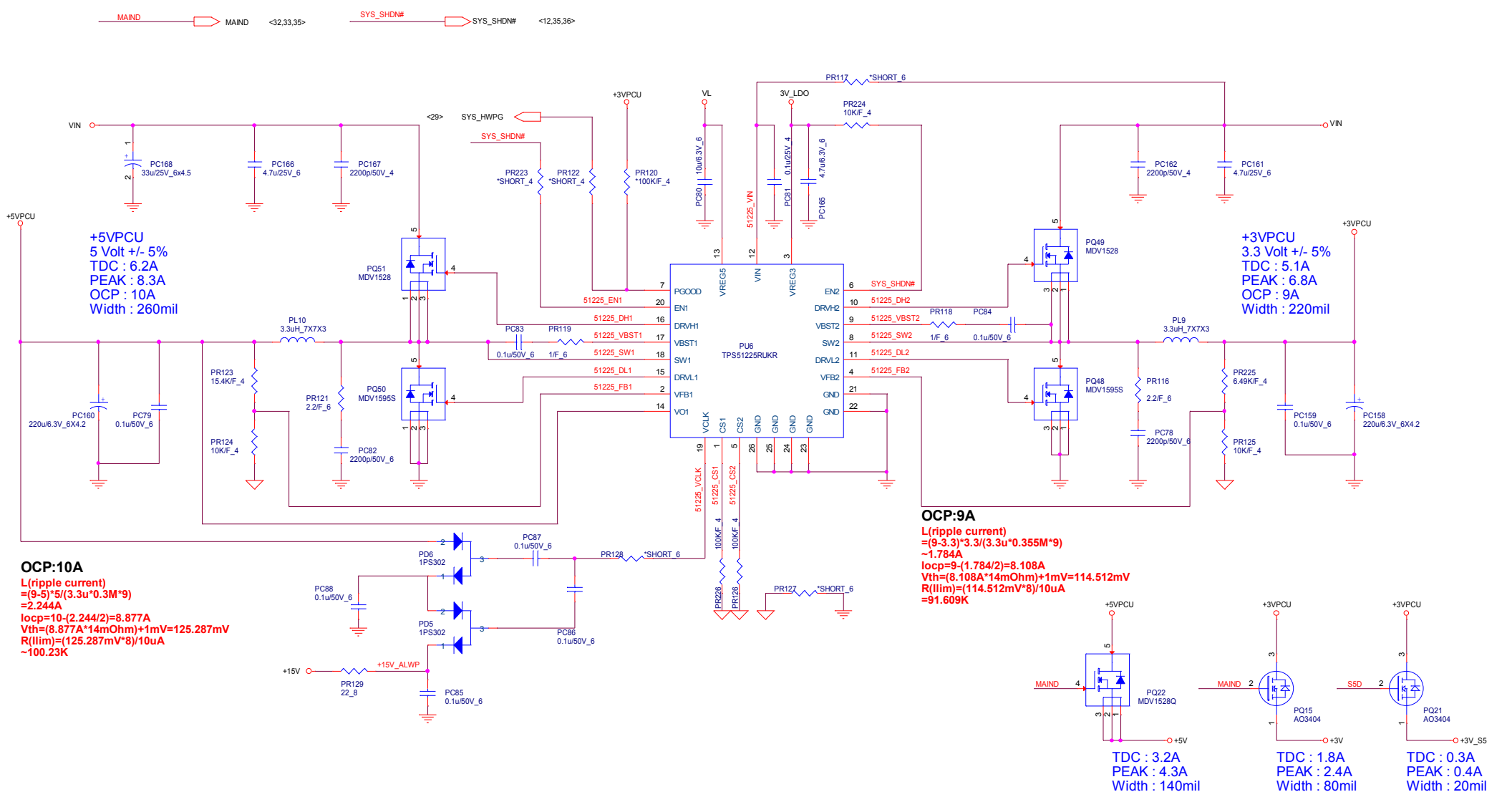


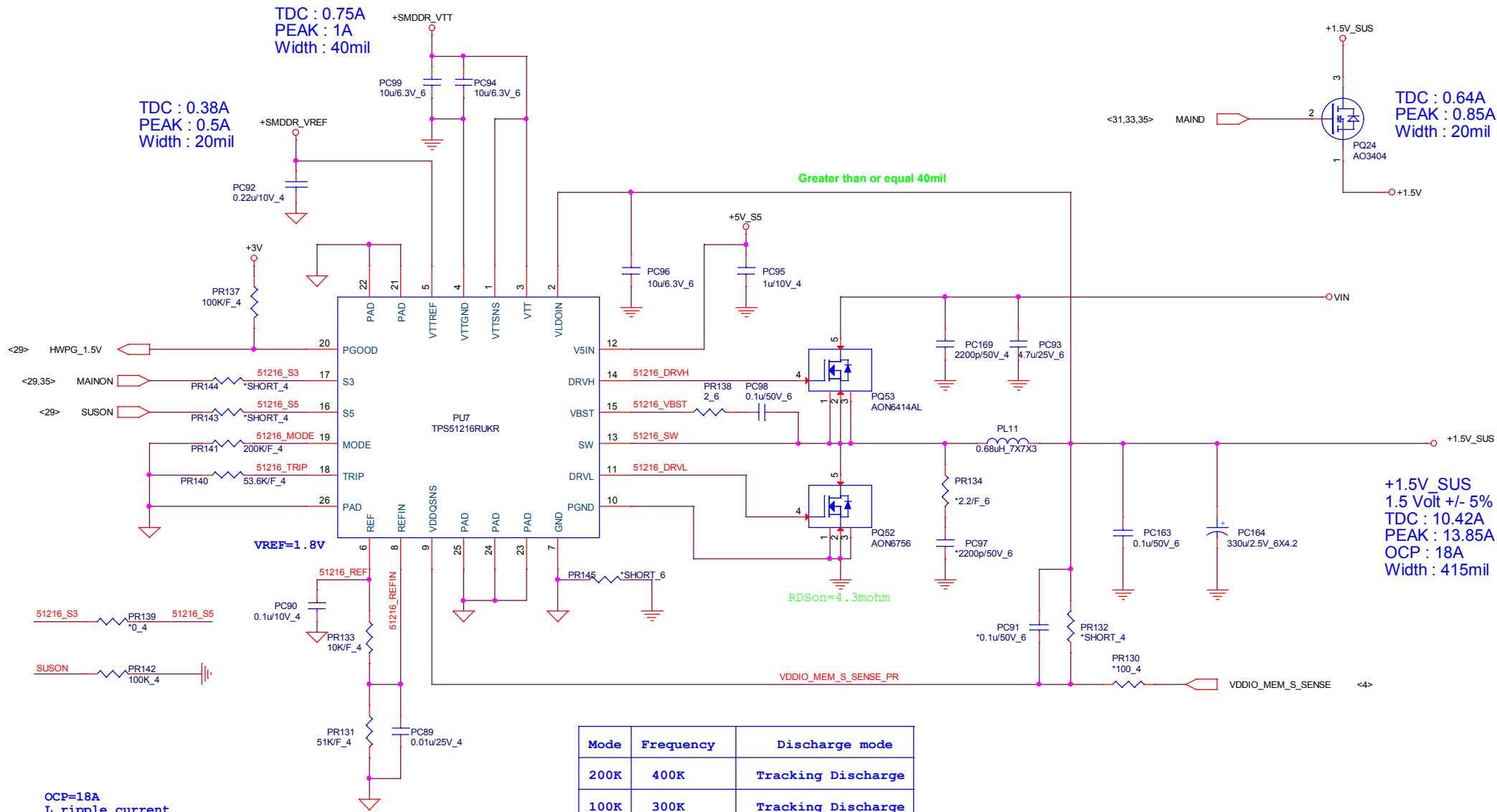
Power sequence

SM BUS ARRANGEMENT TABLE


SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	N/A
SM Bus 4	



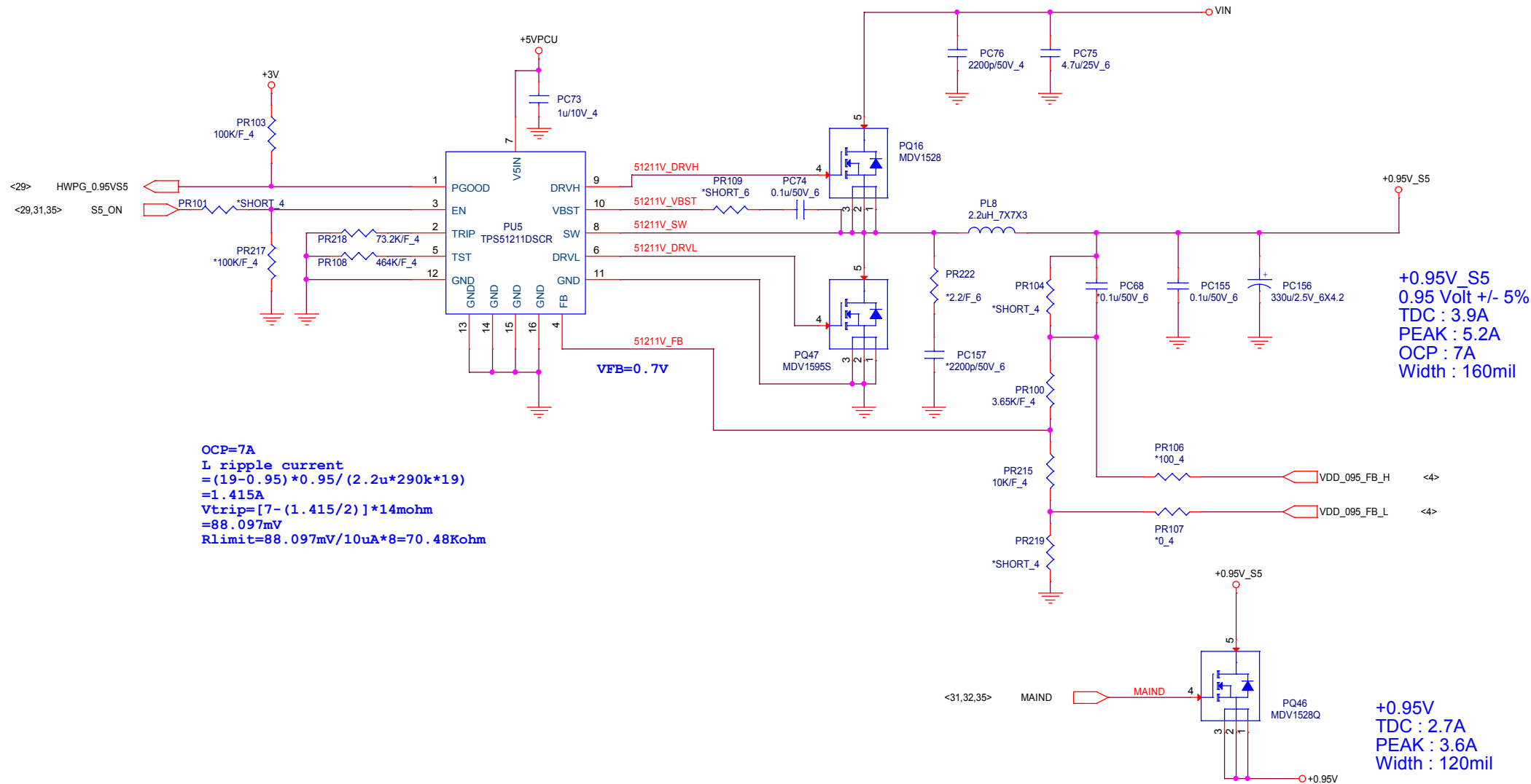




	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF


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PROJECT :

Size	Document Number	Rev
	DDR 1.5V(TPS51216)	1A
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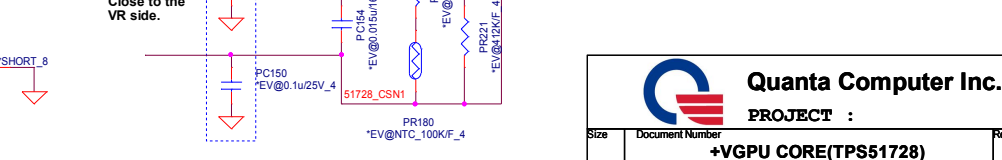
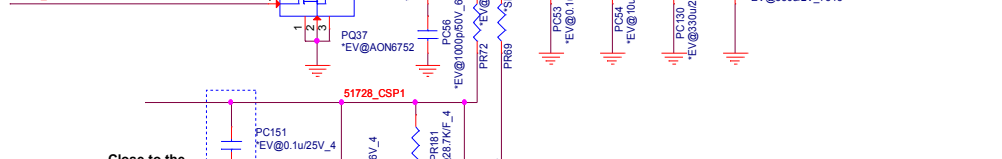
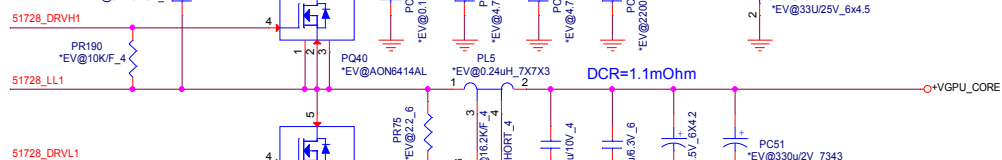
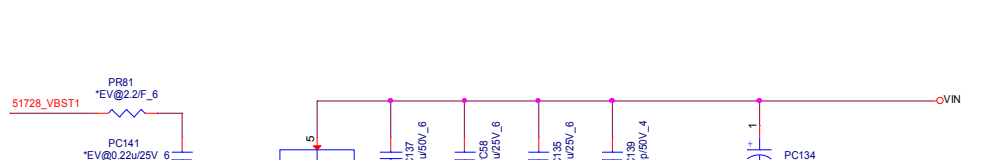
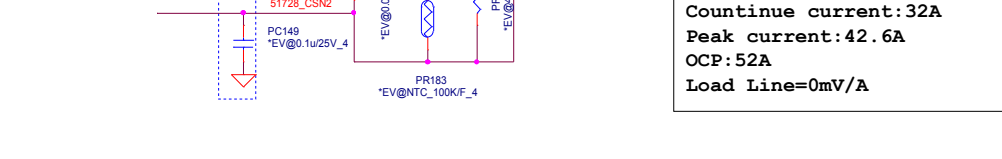
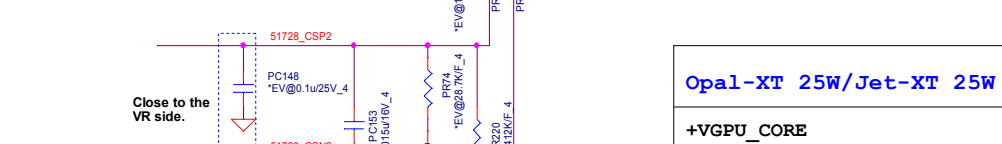
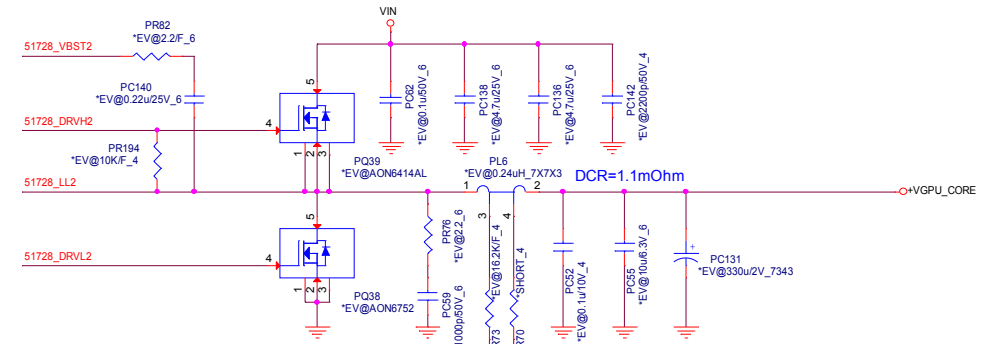
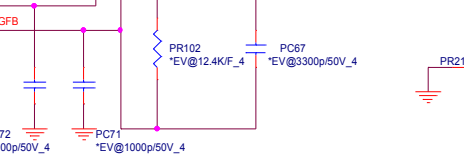
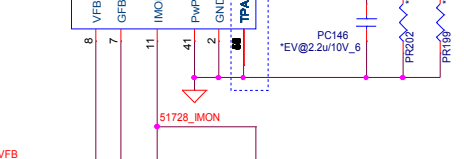
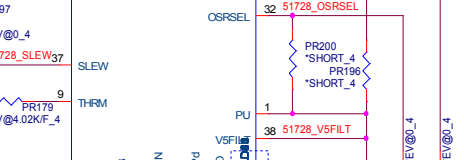
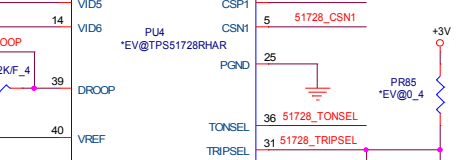
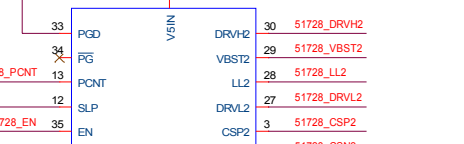
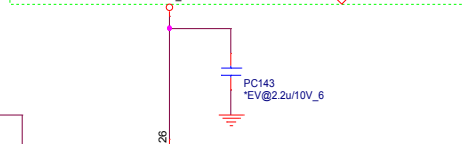
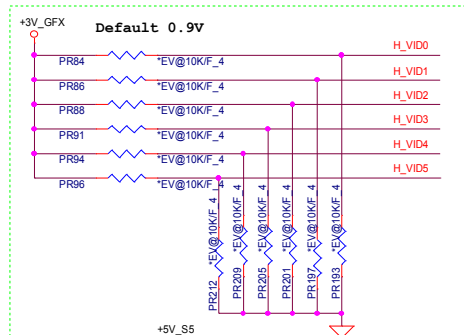
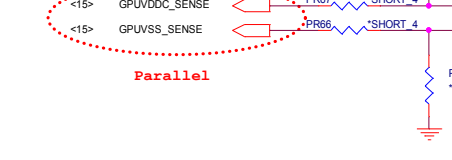
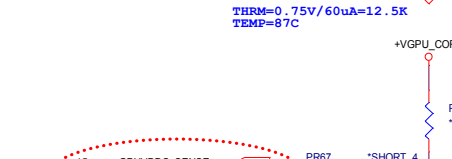
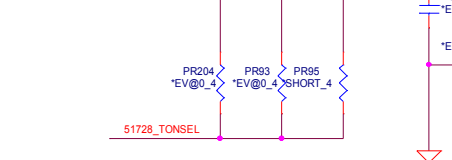
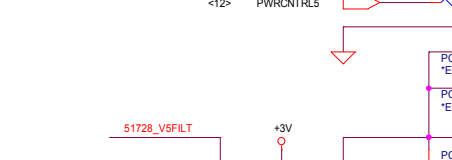
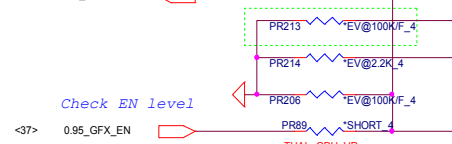
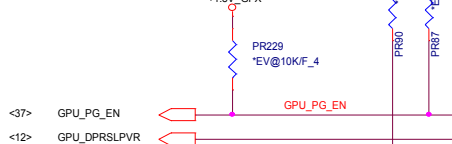
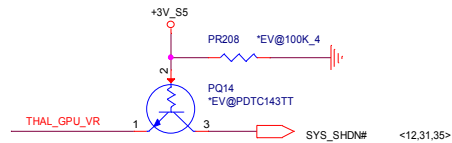


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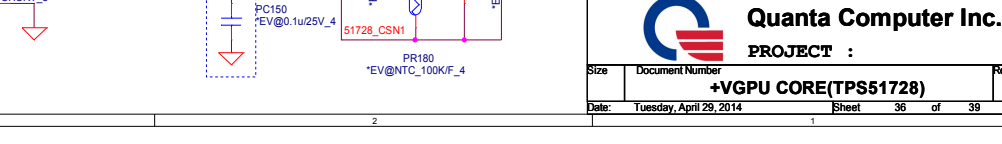
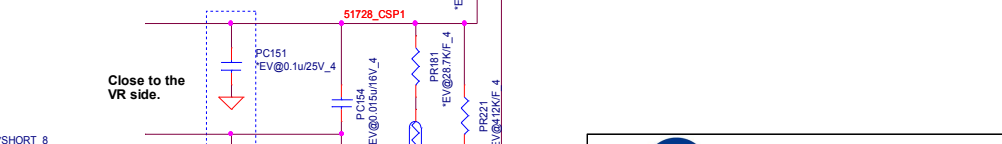
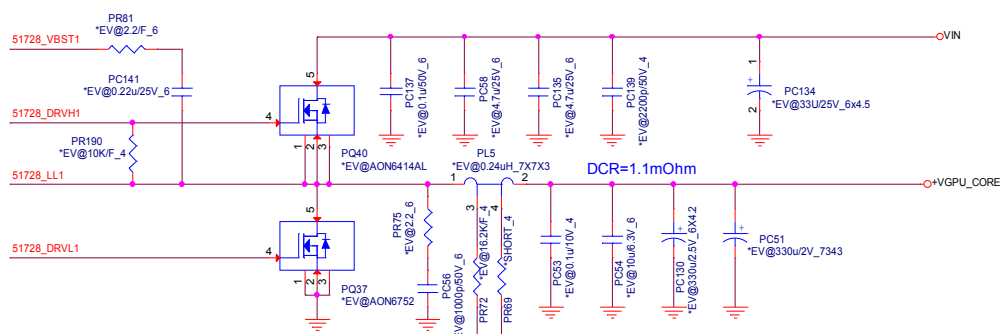
Size	Document Number	Rev
	+0.95V_S5(TPS51211)	1A

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Opal-XT 25W/Jet-XT 25W

+VGPU_CORE
 Countinue current:32A
 Peak current:42.6A
 OCP:52A
 Load Line=0mV/A



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PROJECT : +VGPU CORE(TPS51728)

Size: Document Number: Rev: A1A

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